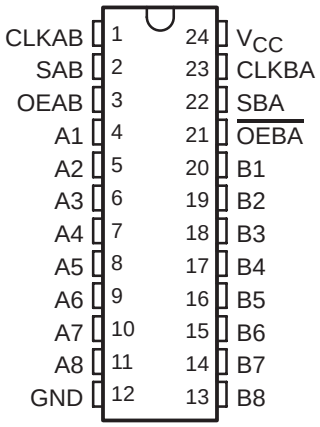
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down To 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)



description/ordering information

This bus transceiver and register is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVTH652 consists of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input selects real-time data and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVTH652 device.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Tape and reel	SN74LVTH652IPWREP	LH652EP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input; therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

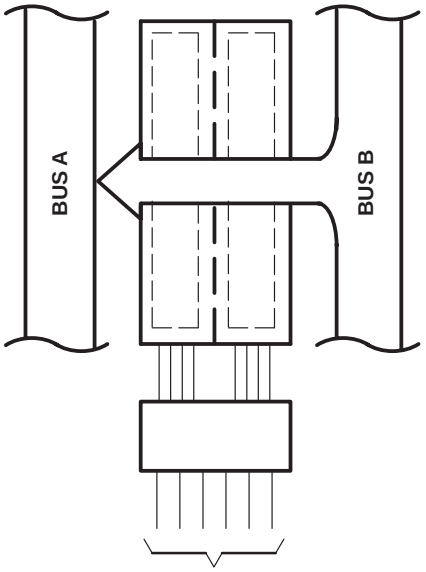
This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1−A8	B1−B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

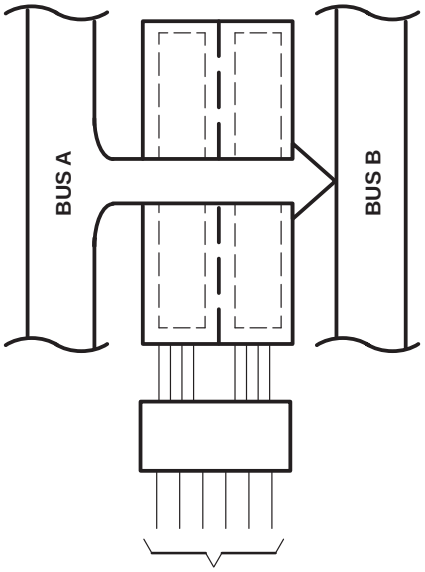
† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.
Select control = H; clocks must be staggered to load both registers.



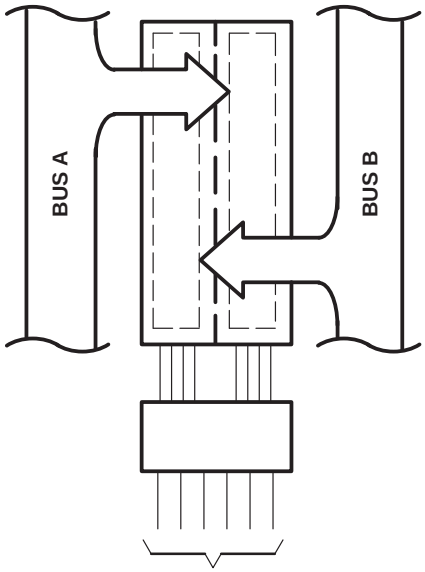
3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



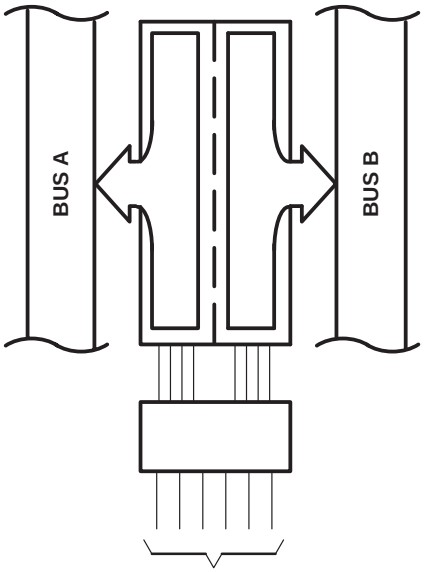
3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

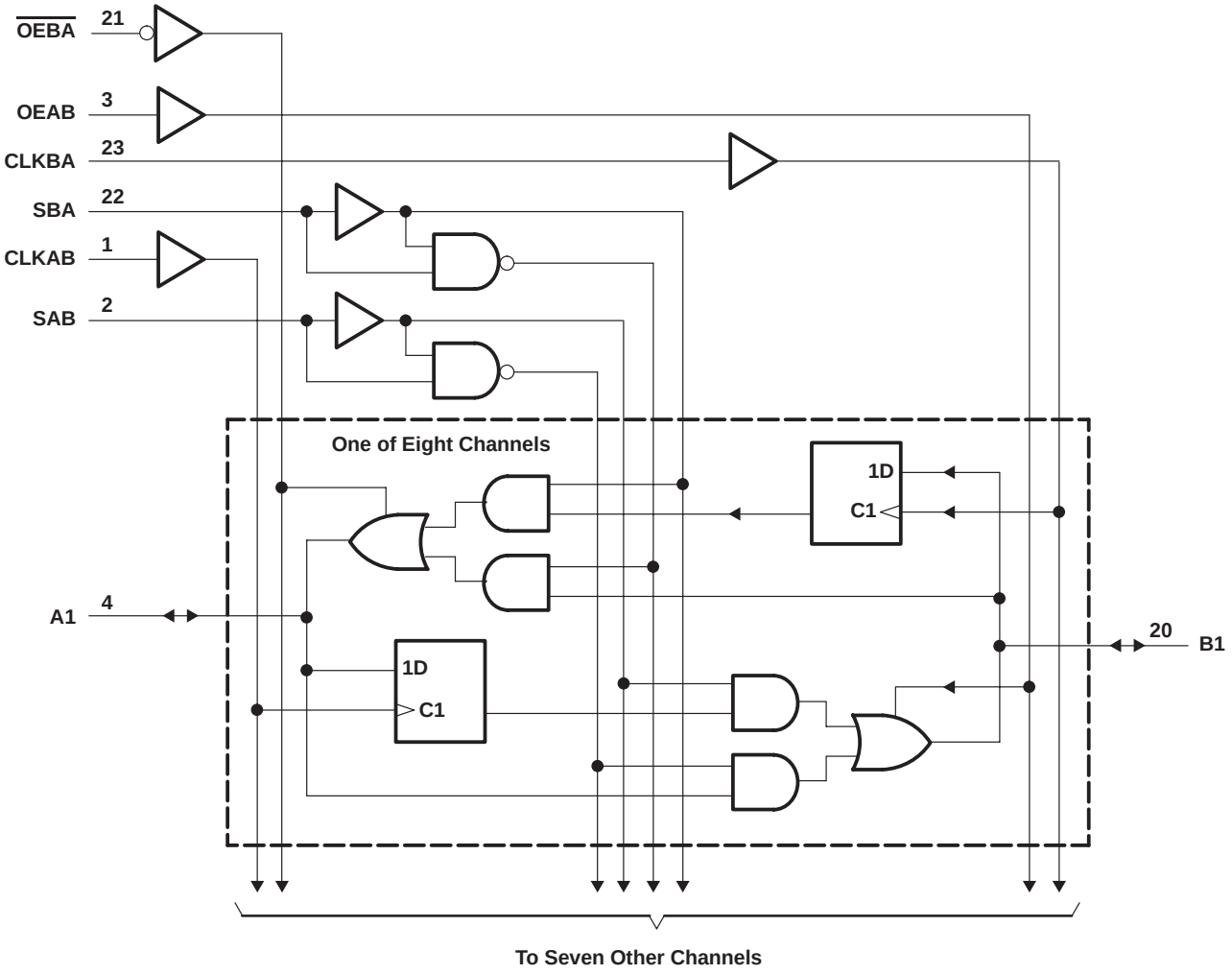


3	21	1	23	2	22
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) . . . . . −0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Current into any output in the high state, I_O (see Note 2) . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 3) . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			−32	mA
I_{OL}	Low-level output current			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		μs/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = −100 μA	V_{CC}−0.2			V
		V_{CC} = 2.7 V,	I_{OH} = −8 mA	2.4			
		V_{CC} = 3 V,	I_{OH} = −32 mA	2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 μA			0.2	V
			I_{OL} = 24 mA			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4	
			I_{OL} = 32 mA			0.5	
			I_{OL} = 64 mA			0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	μA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10	
	A or B ports‡	V_{CC} = 3.6 V	V_I = 5.5 V			20	
			V_I = V_{CC}			1	
			V_I = 0			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			±100	μA
$I_{I(hold)}$	A or B ports	V_{CC} = 3 V	V_I = 0.8 V	75			μA
			V_I = 2 V	−75			
		V_{CC} = 3.6 V§	V_I = 0 to 3.6 V			±500	
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 to 3 V, OE/$\overline{OE}$ = don't care				±100	μA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 to 3 V, OE/$\overline{OE}$ = don't care				±100	μA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19	mA
			Outputs low			5	
			Outputs disabled			0.19	
ΔI_{CC}¶		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2	mA
C_i		V_I = 3 V or 0			4		pF
C_{io}		V_O = 3 V or 0			9		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Unused terminals at V_{CC} or GND
§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

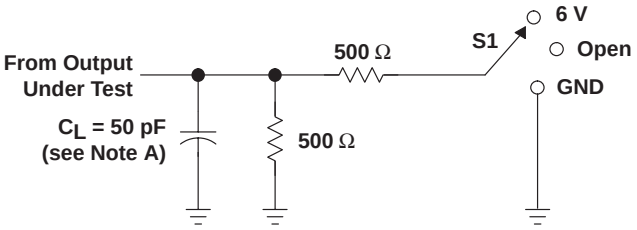
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.2		1.5		ns
		Data low	1.6		2.2		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑		0.8		0.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
f_{max}			150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.8	3.1	4.7		5.6	ns
t_{PHL}			1.8	3.1	4.7		5.6	
t_{PLH}	A or B	B or A	1.3	2.3	3.5		4.1	ns
t_{PHL}			1.3	2.4	3.5		4.1	
t_{PLH}	SBA or SAB‡	A or B	1.5	3.1	4.9		6	ns
t_{PHL}			1.5	3.4	4.9		6	
t_{PZH}	$\overline{OEBA}$	A	1.1	2.9	5.2		6.5	ns
t_{PZL}			1.1	3.1	5.2		6.5	
t_{PHZ}	$\overline{OEBA}$	A	2.3	3.5	5.5		6.1	ns
t_{PLZ}			2.3	3.7	5.5		5.9	
t_{PZH}	OEAB	B	1.3	3	4.7		5.7	ns
t_{PZL}			1.3	3.3	4.7		5.7	
t_{PHZ}	OEAB	B	1.5	3.6	5.6		6.7	ns
t_{PLZ}			1.5	3.7	5.6		6.3	

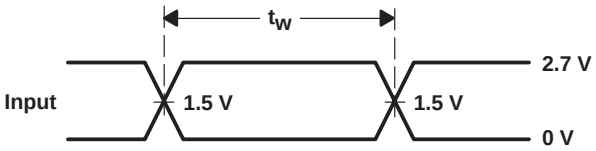
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

PARAMETER MEASUREMENT INFORMATION

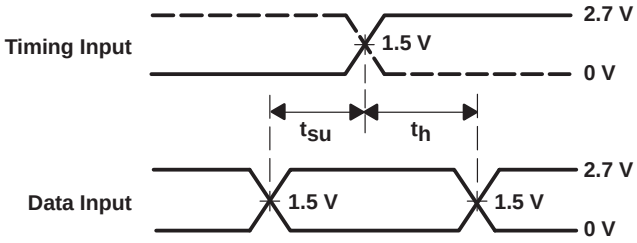


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

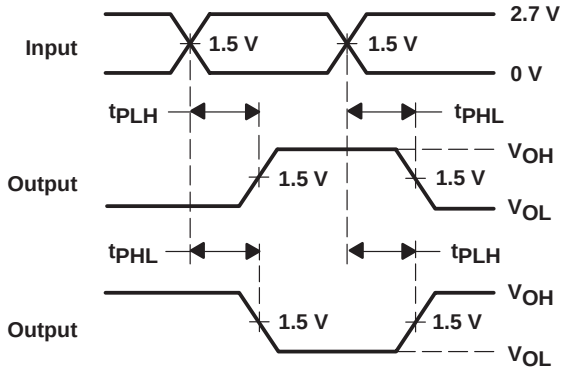
LOAD CIRCUIT



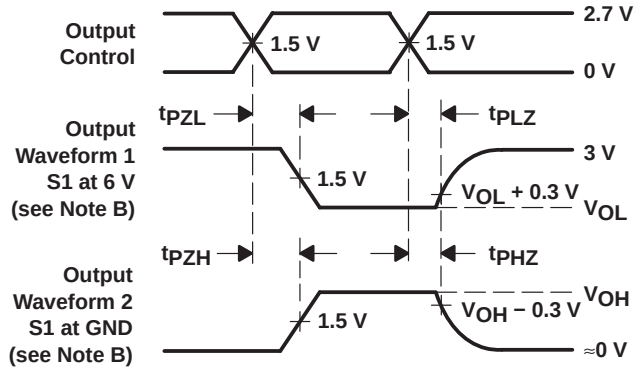
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LVTH652IPWREP	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04681-01XE	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

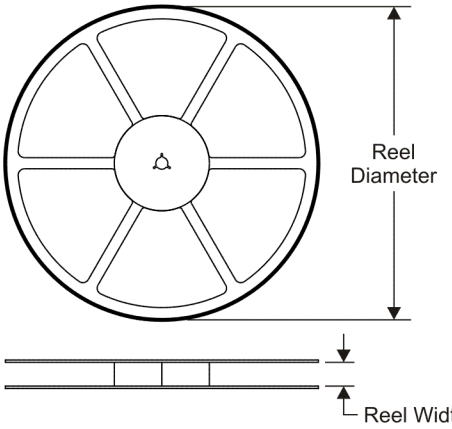
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF SN74LVTH652-EP :
- Catalog: SN74LVTH652

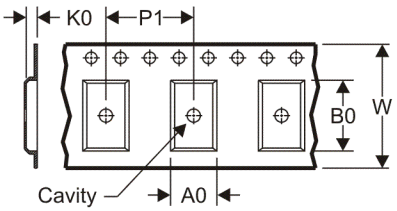
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

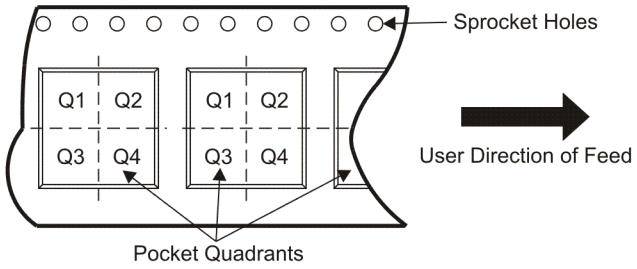


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

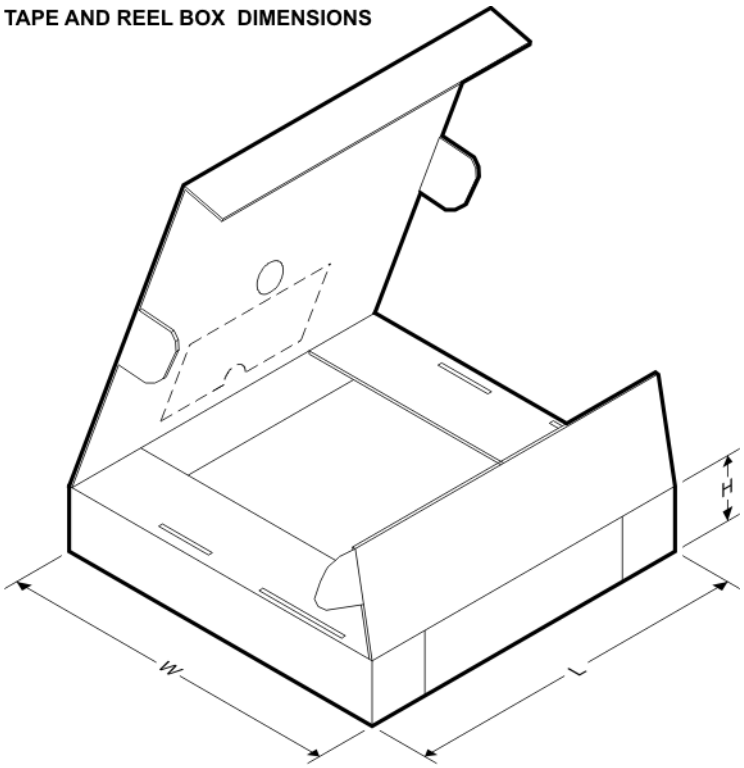
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH652IPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH652IPWREP	TSSOP	PW	24	2000	346.0	346.0	33.0

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