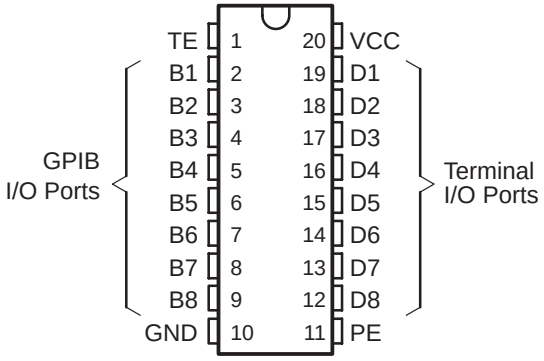
SLLS006A − D2611, OCTOBER 1985 − REVISED FEBRUARY 1993

- **8-Channel Bidirectional Transceivers**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **High-Speed Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 66 mW Max Per Channel**
- **High-impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

DW OR N PACKAGE
(TOP VIEW)



description

NOT RECOMMENDED FOR NEW DESIGN

The SN75163B octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state modes. If talk enable (TE) is high, these outputs have the characteristics of open-collector outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and 400 mV of hysteresis for increased noise immunity.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

The SN75163B is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	H	L
H	X	L	Z
L	H	L	L
X	L	X	Z

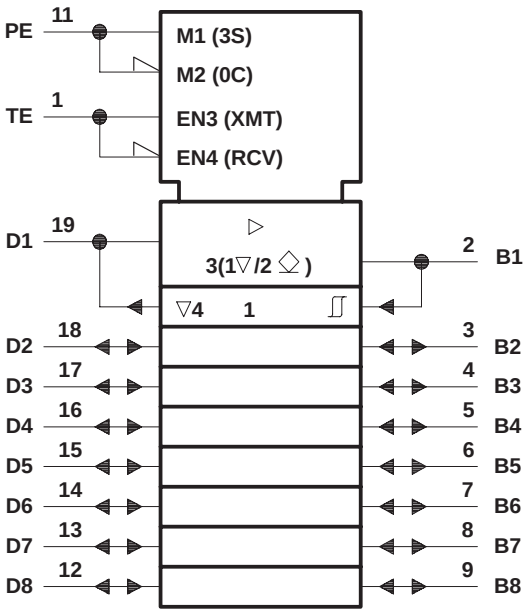
EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = high-impedance state

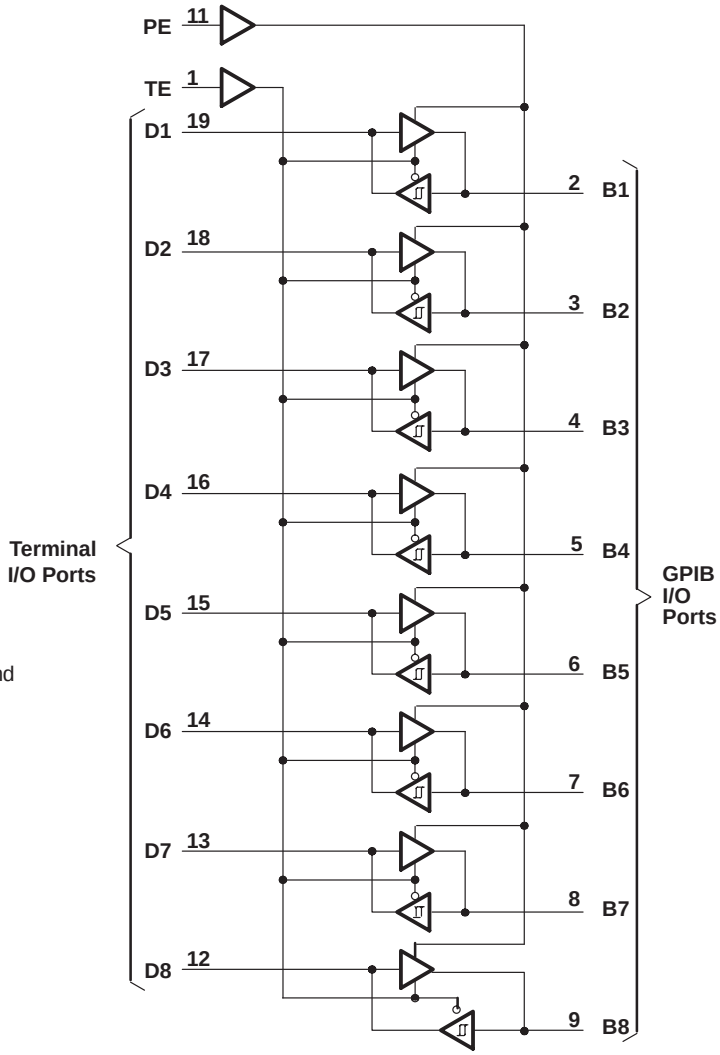
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

logic symbol†



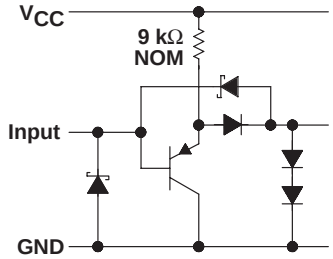
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
◇ Designates open-collector outputs

logic diagram (positive logic)

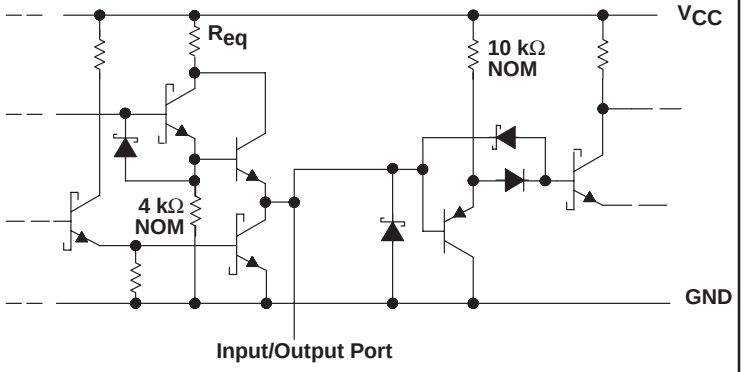


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−10	mA
	Terminal ports			−800	µA
High-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	See Figure 8		0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −10 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	PE and TE at 2 V		0.4	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, PE at 0.8 V, D and TE at 2 V				100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.4 V			−20	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{IL}	Supply current		No load	Receivers low and enabled			80	mA
				Drivers low and enabled			100	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

† All typical values are at V_{CC} = 5, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pullup enable time	PE	Terminal	See Figure 5		15	22	ns
t_{dis}	Output pullup disable time					13	20	

PARAMETER MEASUREMENT INFORMATION

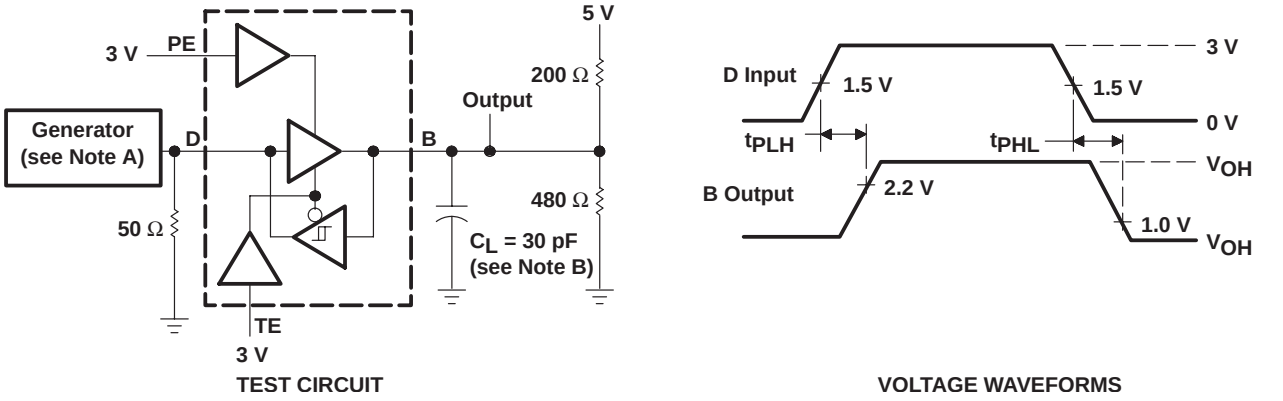

Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

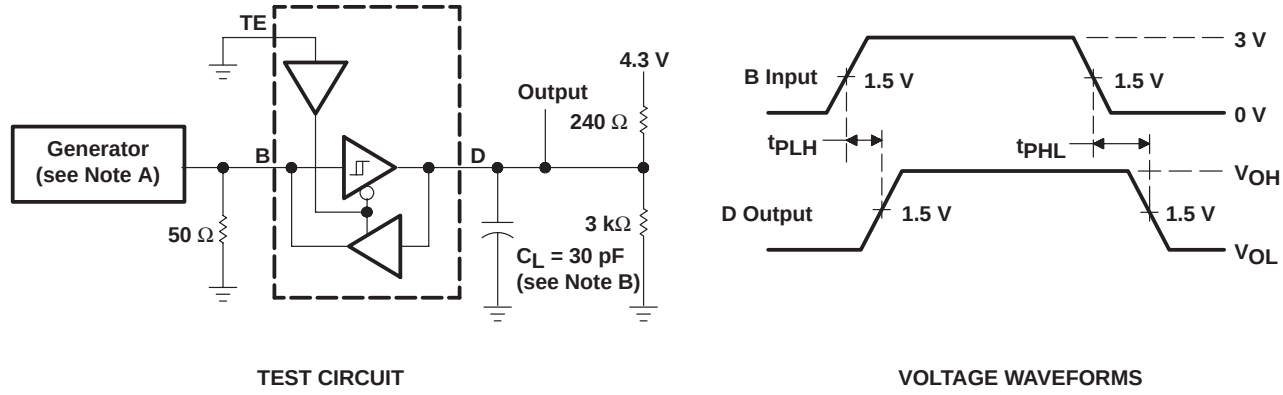

Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

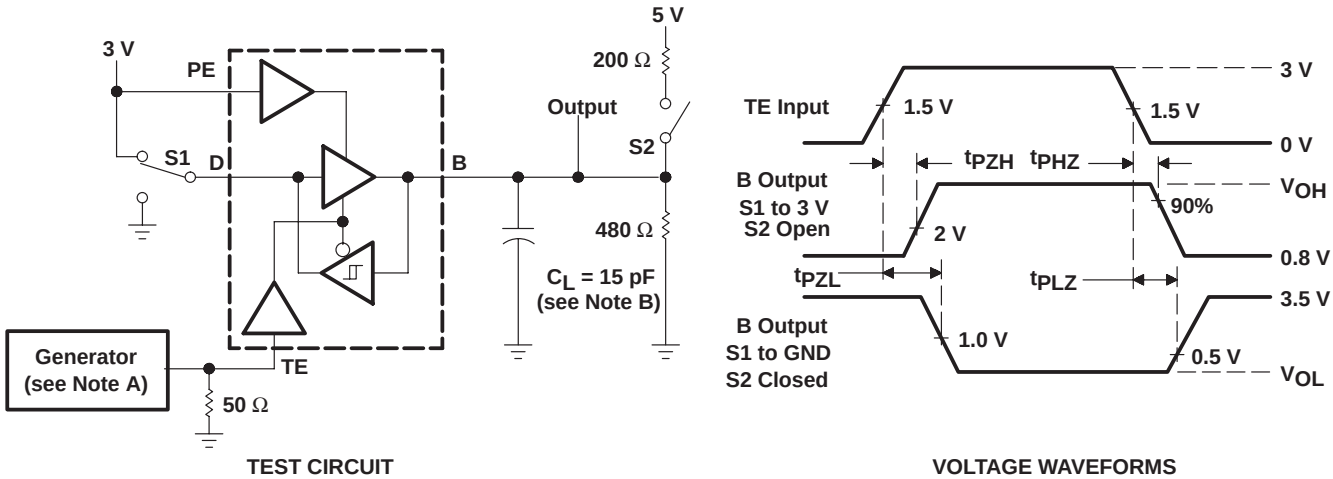

Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

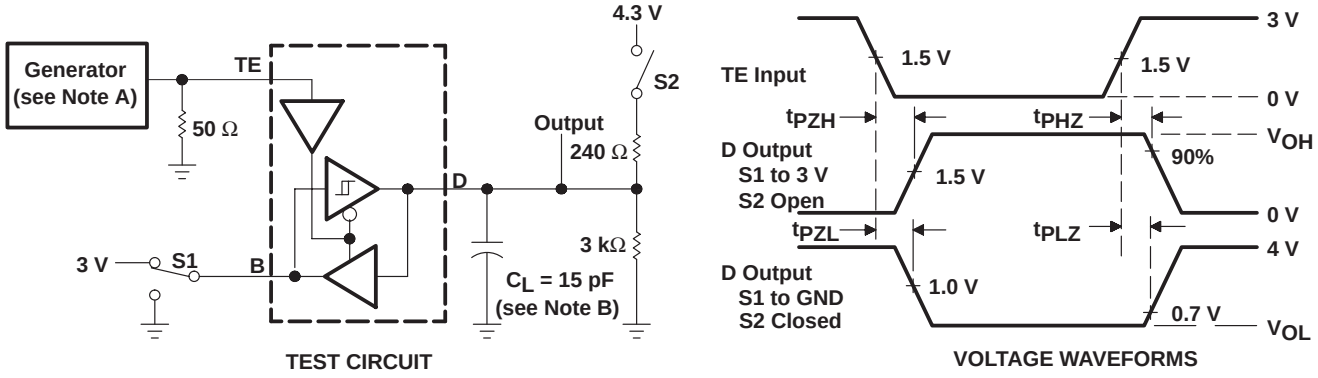

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

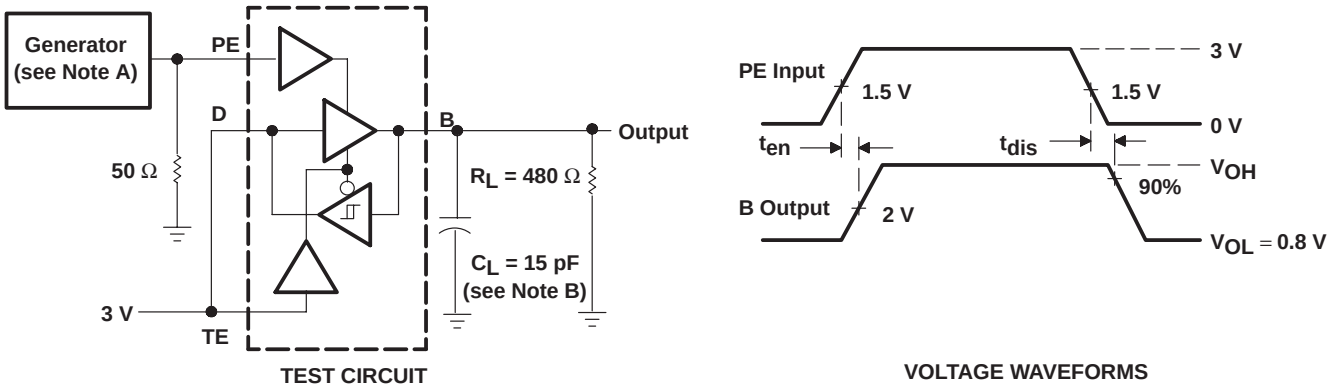

Figure 5. PE-to-Bus Pullup Test Circuit and Voltage Waveforms

NOTES: C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
D. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

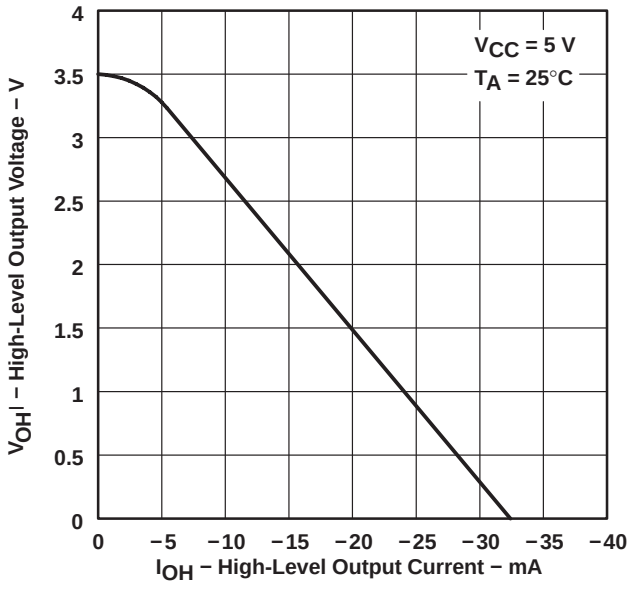

Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

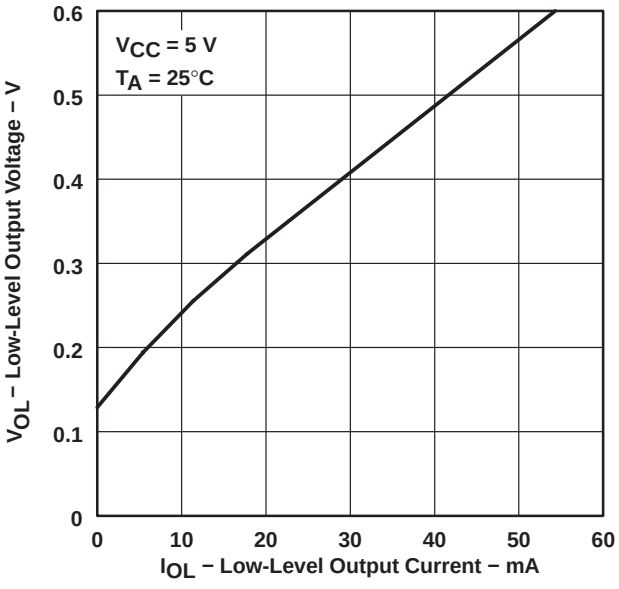

Figure 7

TERMINAL OUTPUT VOLTAGE vs BUS INPUT VOLTAGE

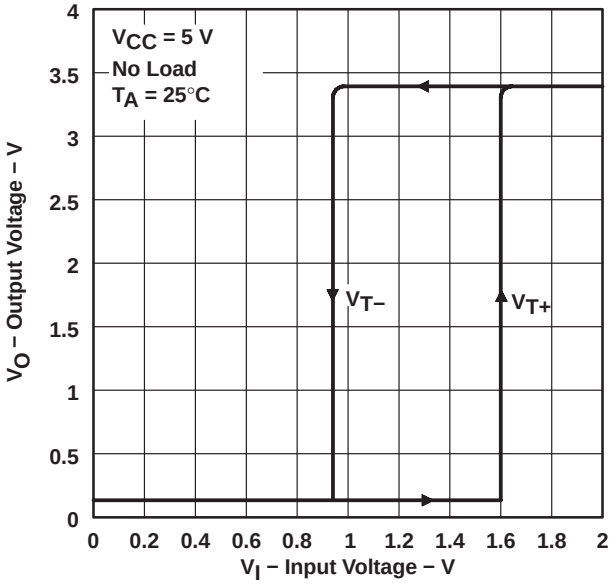

Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

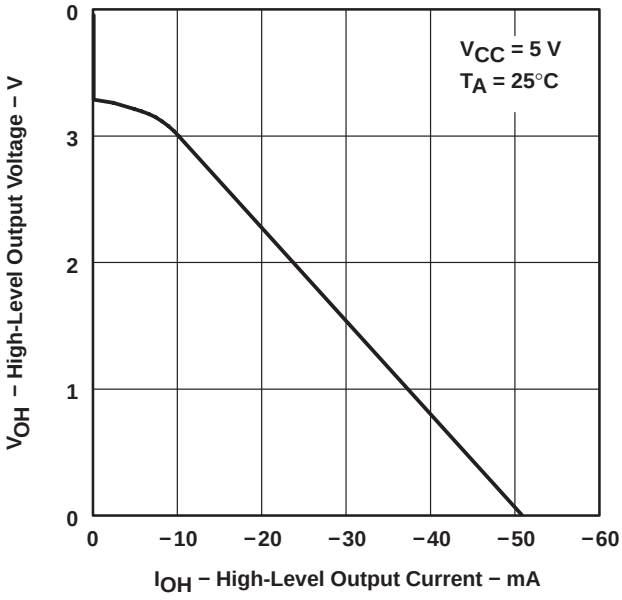

Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

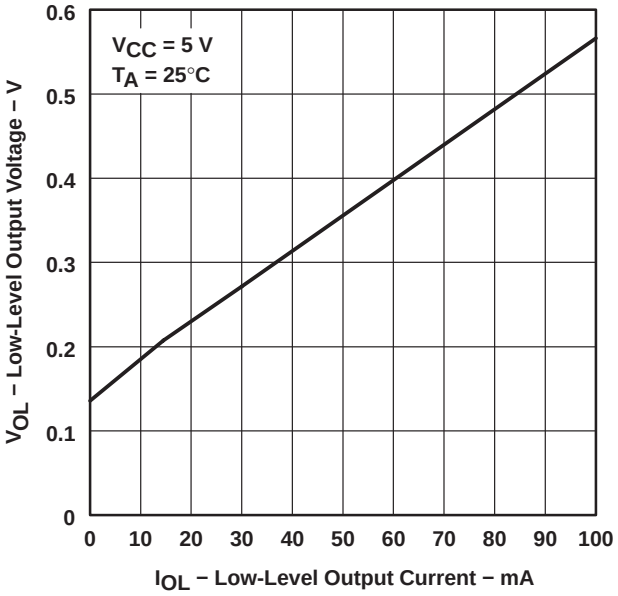

Figure 10

BUS OUTPUT VOLTAGE vs THERMAL INPUT VOLTAGE

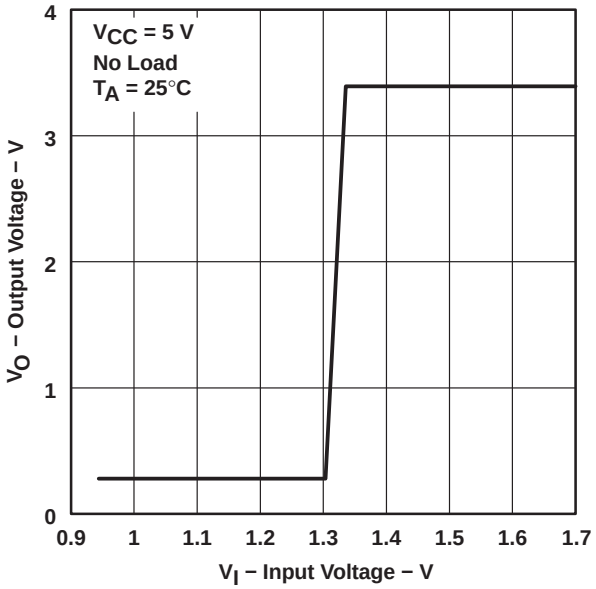

Figure 11

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