signetics DUAL CORE MEMORY SENSE AMPLIFIERS

SN7520
SN7521
SN7522
SN7523
SN7524
SN7525

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The 7520 Series Dual Core Memory Sense Amplifiers are designed for use in high speed core memory systems. Three separate logic configurations allow flexibility of system design.

The 7520 and 7521 can be used to perform the function of a flip-flop or a data register which responds to the sense and strobe-input conditions.

The 7522 and 7523 features an open collector stage which may be used to perform the wired-OR function.

The 7524 and 7525 features two independent sense channels with separate outputs.

FEATURES

- DUAL SENSE AMPS
- ±4mV THRESHOLD UNCERTAINTY
- DESIGN VERSATILITY
- 25ns PROPAGATION DELAY

ABSOLUTE MAXIMUM RATINGS

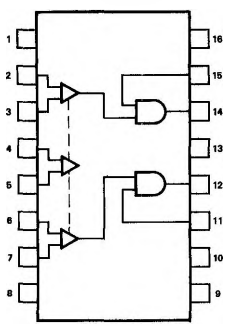
Differential Input Voltage	±5V
V_{CC}	±7V
Strobe & Gain Input Voltages	+5.5V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation	500mW

PIN CONFIGURATIONS

B PACKAGE (Top View)

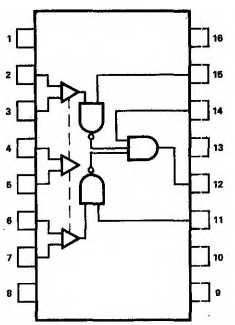
7520/21

ORDER PART NOS.
SN7520N/
SN7521N



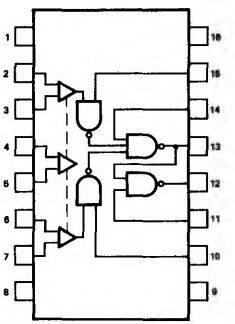
7522/23

ORDER PART NOS.
SN7522N/
SN7523N



7524/25

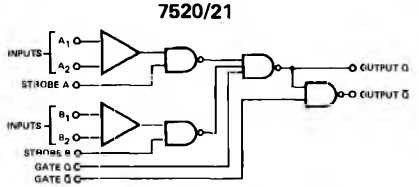
ORDER PART NOS.
SN7524N/
SN7525N



*The Signetics 7520/21/22/23/24/25 does not require an external capacitor (C_{ext}) to stabilize the pre-amplifier. Pin 1 may be used as a test point, giving access to the pre-amplifier output. No degradation of performance will result if a 100pF capacitor is connected from Pin 1 to GND.

LOGIC DIAGRAMS

7520/21



$\underline{\text{Output } Q} = \overline{G_Q} + (S_A\ IN_A + S_B\ IN_B)\ G_Q$

$\underline{\text{Output } \overline{Q}} = G_Q\ (\overline{G_Q} + S_A\ IN_A + S_B\ IN_B)$

where:

G_Q = Gate Q ≥ 2V

S_A = Strobe A ≥ 2V

IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

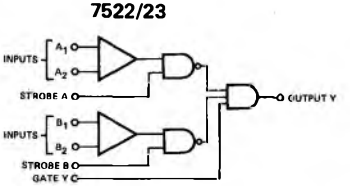
S_B = Strobe B ≥ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

$\overline{G_Q}$ = Gate Q ≤ 0.8V

$G_{\overline{Q}}$ = Gate $\overline{Q}$ ≥ 2V

7522/23



$\underline{\text{Output } Y} = G(S_A\ IN_A + S_B\ IN_B) + \overline{G}$

where:

G = Gate ≥ 2V

S_A = Strobe A ≥ 2V

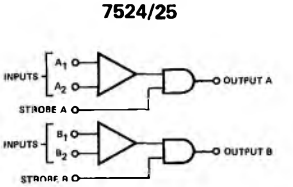
IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

S_B = Strobe B ≥ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

G = Gate ≤ 0.4V

7524/25



Output A = $S_A\ IN_A$

Output B = $S_B\ IN_B$

where:

S_A = Strobe A ≥ 2V

IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

S_B = Strobe B ≥ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_T	Differential-Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7520	11	15	18	mV
			7521	8	15	22	mV
		V_{ref} = 40mV	7520	36	40	44	mV
			7521	33	40	47	mV
		Strobe Input: $V_{inS} = V_{in(1)}$					
V_{CMF}	Common-Mode Input Firing Voltage (See Note 2)	Common-Mode Input Pulse: $t_r = t_f \leq 15ns$, $t_{p(in)}$ = 50ns T_A = 25°C			±3		V
I_{in}	Differential-Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential-Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential-Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (gate	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA			0.25	0.4	V
$I_{OS(Q)}$	Q Output Short-Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		3.3		5	mA
$I_{OS(\overline{Q})}$	$\overline{Q}$ Output Short-Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			28		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			-14		mA
$t_{or\ D}$	Differential-Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or\ CM}$	Common-Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum cycle time				200		ns

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)DQ}$, $t_{pd(0)DQ}$	$A_1 - A_2$ or $B_1 - B_2$	Q		20 30	40	ns ns
$t_{pd(1)D\overline{Q}}$, $t_{pd(0)D\overline{Q}}$	$A_1 - A_2$ or $B_1 - B_2$	$\overline{Q}$		25 35	 55	ns ns
$t_{pd(1)SQ}$, $t_{pd(0)SQ}$	Strobe A or B	Q		15 25	30	ns ns
$t_{pd(1)S\overline{Q}}$, $t_{pd(0)S\overline{Q}}$	Strobe A or B	$\overline{Q}$		15 35	 55	ns ns
$t_{pd(1)G_QQ}$, $t_{pd(0)G_QQ}$	Gate Q	Q		10 15	20	ns ns
$t_{pd(1)G_Q\overline{Q}}$, $t_{pd(0)G_Q\overline{Q}}$	Gate Q	$\overline{Q}$		15 20	 30	ns ns
$t_{pd(1)G_Q\overline{Q}}$, $t_{pd(0)G_Q\overline{Q}}$	Gate $\overline{Q}$	$\overline{Q}$		15 10	 20	ns ns

(SEE NOTES PAGE 128)

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Differential Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7522	11	15	19	mV
			7523	8	15	22	mV
		V_{ref} = 40mV	7522	36	40	44	mV
			7523	33	40	47	mV
V_{CMF}	Common Mode Input Firing Voltage (See Note 2)	Strobe Input: $V_{inS} = V_{in(1)}$ Common Mode Input Pulse: $t_r = t_f \geq 15ns$, $t_{p(in)} = 50ns$ $T_A = 25°C$			±3		V
I_{in}	Differential Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V			-1	-1.6	mA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
$I_{in(1)}$	Logical 1 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA, V_{in} = 2V		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA, V_{in} = 0.8V			0.2	0.4	V
$I_{out(1)}$	Output Reverse Current	V_{cc1} = 4.75V, V_{cc2} = -4.75V V_{out} = 5.25V, V_{in} = 2V				250	μA
I_{OS}	Output Short Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			27		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			15		mA
$t_{or D}$	Differential Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or CM}$	Common Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = ±2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum Cycle Time				200		ns

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)D}$	$A_1 - A_2$ or $B_1 - B_2$	Y		20		ns
$t_{pd(0)D}$				30	45	ns
$t_{pd(1)S}$	Strobe A or B	Y		15		ns
$t_{pd(0)S}$				25	40	ns
$t_{pd(1)G}$	Gate	Y		10		ns
$t_{pd(0)G}$				15	25	ns

(SEE NOTES PAGE 128)

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Differential Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7524	11	15	19	mV
			7525	8	15	22	mV
		V_{ref} = 40mV	7524	36	40	44	mV
			7525	33	40	47	mV
		Strobe Input: $V_{inS} = V_{in(1)}$					
V_{CMF}	Common Mode Input Firing Voltage (See Note 2)	Common Mode Input Pulse: $t_r = t_f \leq 15ns$, $t_{p(in)} = 50ns$ $T_A = 25°C$			±3		V
I_{in}	Differential Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V			-1	-1.6	mA
$I_{in(1)}$	Logical 1 Level Input Current (strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA, $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA, $V_{in(0)}$ = 0.8V			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			25		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			-15		mA
$t_{or D}$	Differential Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or CM}$	Common Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = ±2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum Cycle Time				200		ns

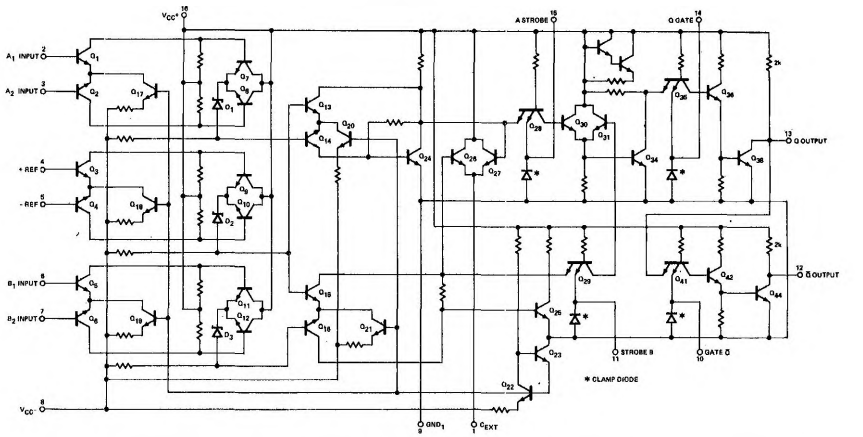
PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)D}$	$A_1 - A_2$ or $B_1 - B_2$	A or B		25	40	ns
$t_{pd(0)D}$				20		ns
$t_{pd(1)S}$	Strobe A or B	A or B		15	30	ns
$t_{pd(0)S}$				20		ns

NOTES:

1. The differential input threshold voltage (V_T) is defined as the DC input voltage (V_{in}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
2. Common mode input firing voltage is the common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable signal present.
3. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
4. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

SCHEMATIC DIAGRAMS

7520/21



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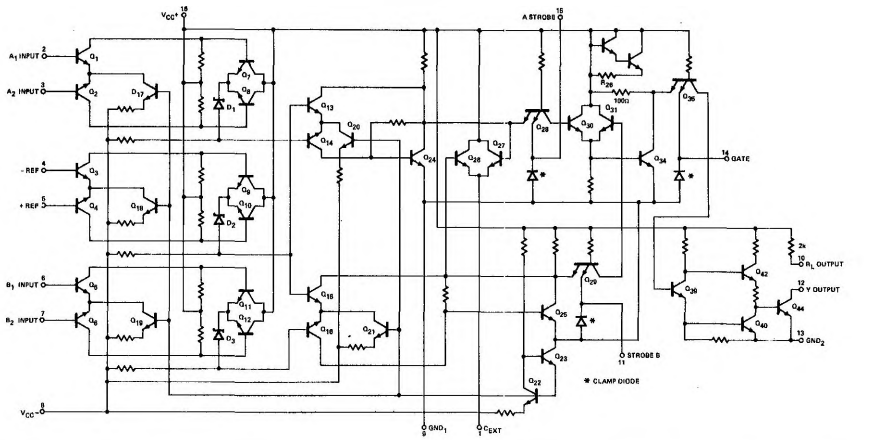
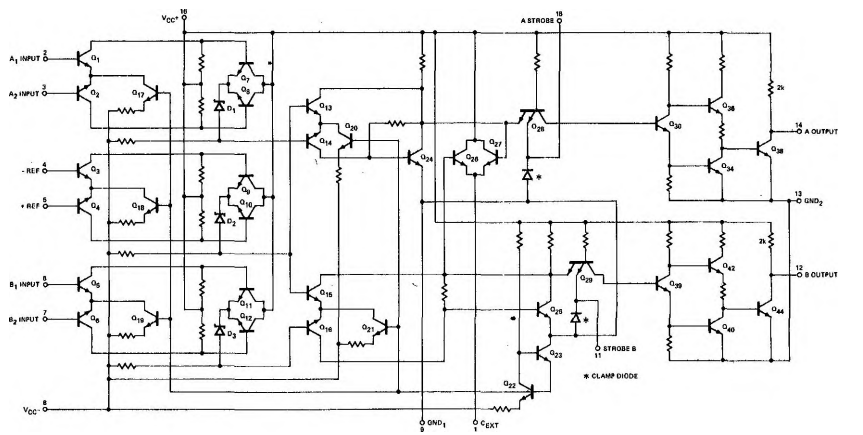
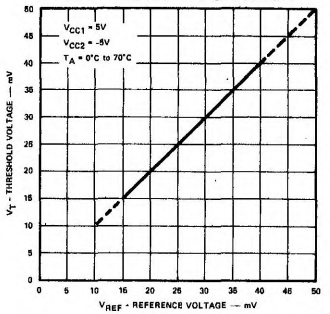


7524/25

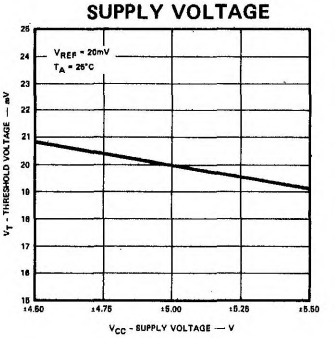


TYPICAL CHARACTERISTIC CURVES

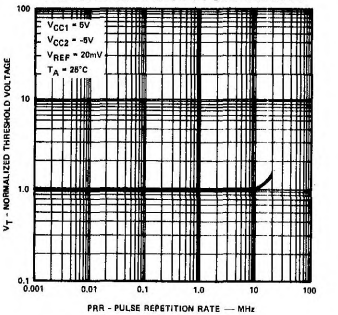
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



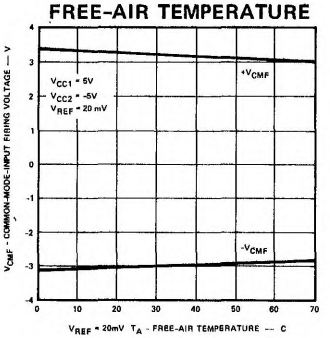
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



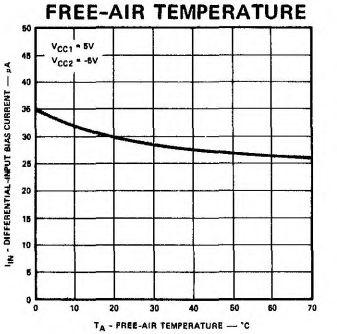
NORMALIZED THRESHOLD VOLTAGE VERSUS PULSE REPETITION RATE



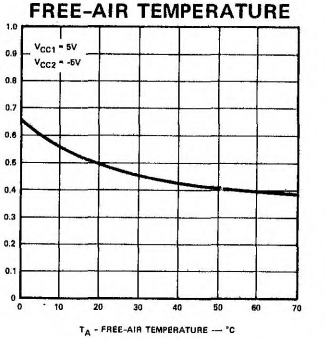
COMMON-MODE FIRING VOLTAGE VERSUS FREE-AIR TEMPERATURE



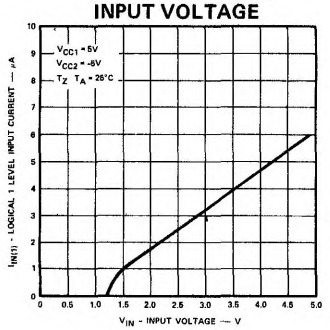
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



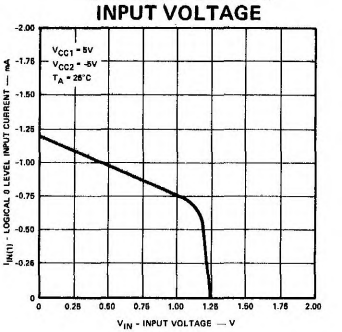
DIFFERENTIAL-INPUT OFFSET CURRENT VS FREE-AIR TEMPERATURE



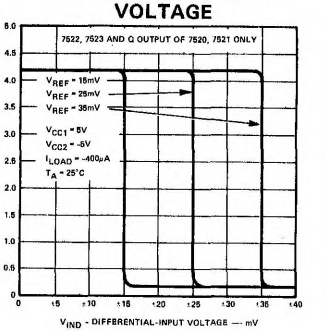
LOGICAL 1 LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



LOGICAL 0 LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE

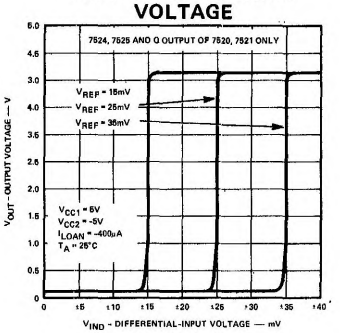


OUTPUT VOLTAGE VERSUS DIFFERENTIAL-INPUT VOLTAGE

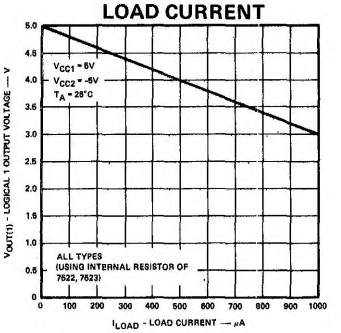


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

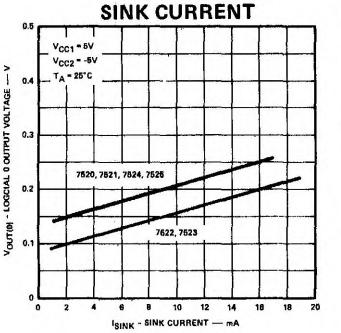
OUTPUT VOLTAGE VERSUS DIFFERENTIAL-INPUT VOLTAGE



LOGICAL 1 OUTPUT VOLTAGE VERSUS LOAD CURRENT



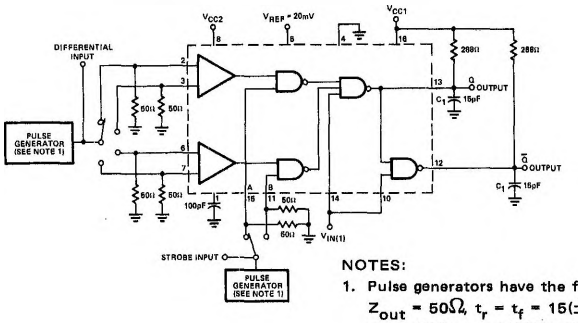
LOGICAL 0 OUTPUT VOLTAGE VERSUS SINK CURRENT



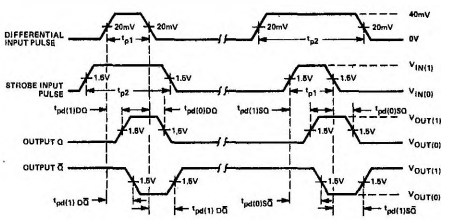
SWITCHING CHARACTERISTICS (Propagation Delay Times)

TEST CIRCUIT — DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS

7520/21



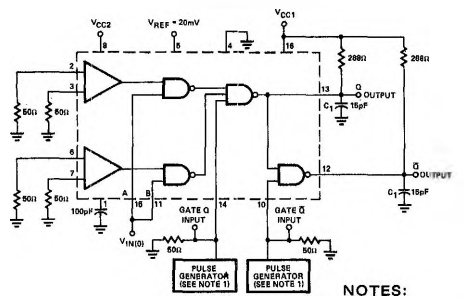
VOLTAGE WAVEFORMS — DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS



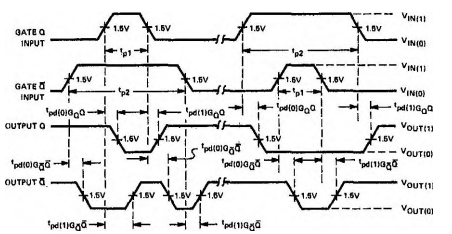
NOTES:

1. Pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 15(\pm5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, and PRR = 1 MHz.
2. C_1 includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS



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SWITCHING CHARACTERISTICS (Propagation Delay Times)(Cont'd)

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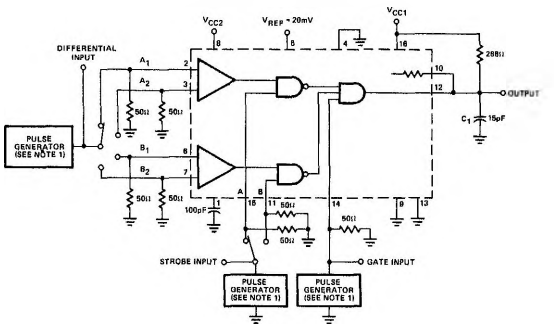
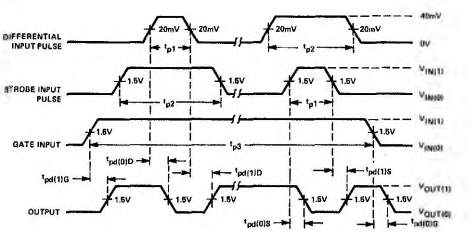
TEST CIRCUIT



VOLTAGE WAVEFORMS



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   t_{p2} = 300ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs $A_1 - A_2$ are being tested and to Strobe B when inputs $B_1 - B_2$ are being tested.
3. C_1 includes probe and jig capacitance.

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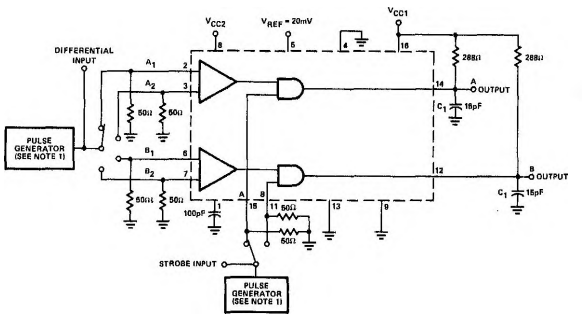
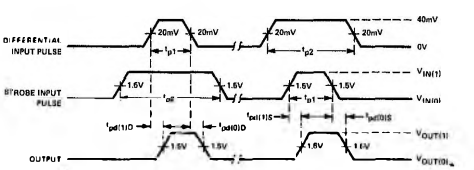
TEST CIRCUIT



VOLTAGE WAVEFORMS



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