

SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

SLLS010D – JUNE 1986 – REVISED MAY 1995

- Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A
- Meet ITU Recommendations V.10 and V.11
- Designed to Operate Up to 20 Mbaud
- -7 V to 7 V Common-Mode Input Voltage Range With 200-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 k Ω Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement
35 mA Max
- Improved Speed and Power Consumption Compared to MC3486

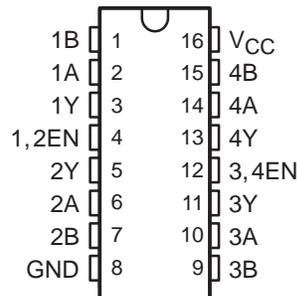
description

The SN55ALS195 and SN75ALS195 are four differential line receivers with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

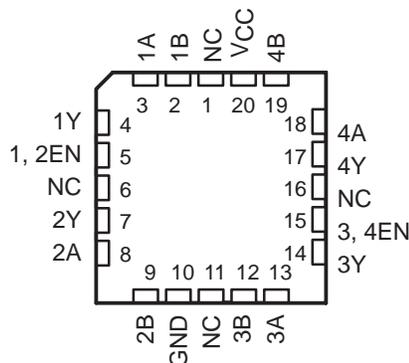
The devices are optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of ± 7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

The SN55ALS195 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75ALS195 is characterized for operation from 0°C to 70°C .

SN55ALS195 . . . J OR W PACKAGE
SN75ALS195 . . . J OR N PACKAGE†
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
† For surface-mount package, see the SN75ALS199.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

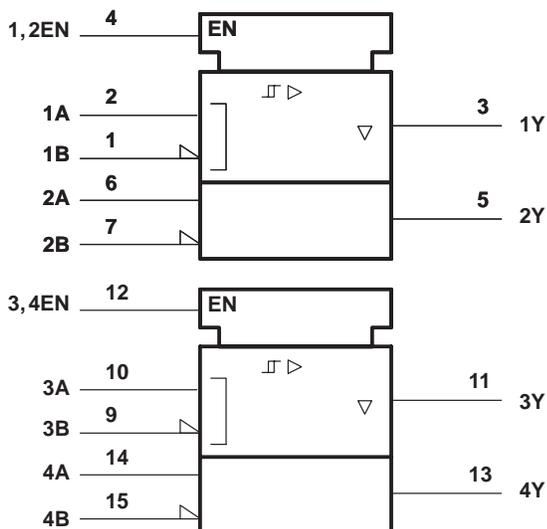
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FUNCTION TABLE
(each receiver)

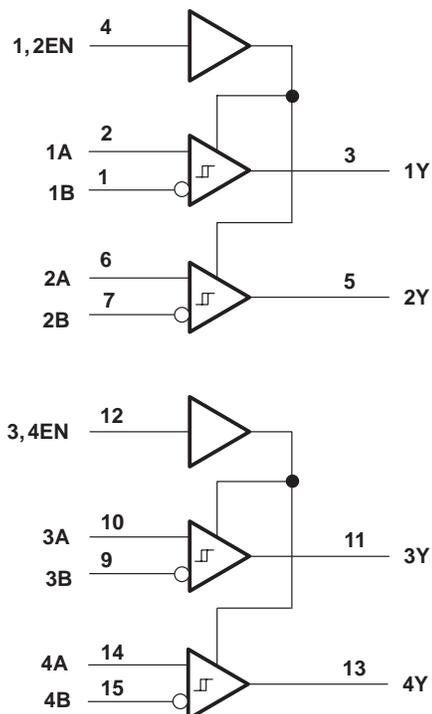
DIFFERENTIAL INPUTS A-B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2V$	H	H
$-0.2V < V_{ID} < 0.2V$	H	?
$V_{ID} \leq -0.2V$	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

logic symbol†



logic diagram



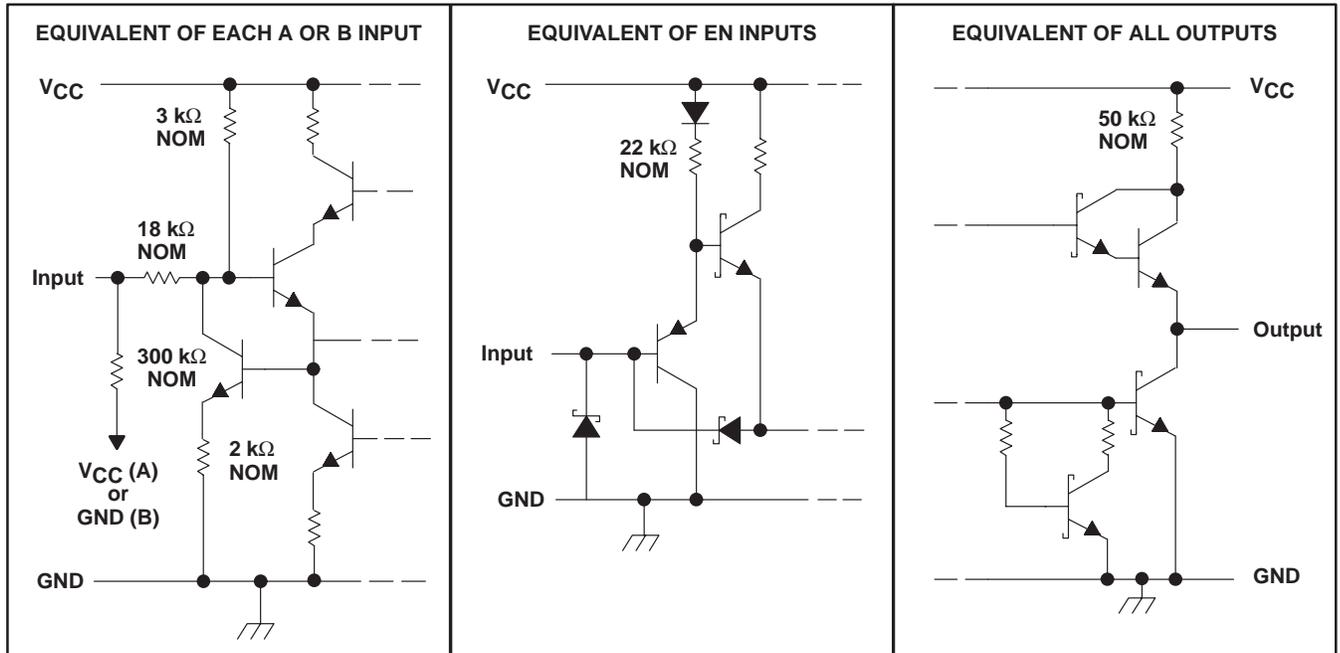
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J, N, and W packages.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage, A or B inputs, V _I	±15 V
Differential input voltage, V _{ID} (see Note 2)	±15 V
Enable input voltage, V _I	7 V
Low-level output current, I _{OL}	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T _A : SN55ALS195	–55°C to 125°C
SN75ALS195	0°C to 70°C
Storage temperature range, T _{stg}	–65°C to 150°C
Case temperature for 60 seconds, T _C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, N, or W package	300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 125°C POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2 mW/°C	656 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

SN55ALS195, SN75ALS195 QUADRUPLE DIFFERENTIAL LINE RECEIVERS

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recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}	±7			±7			V
Differential input voltage, V_{ID}	±12			±12			V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}	0.8			0.8			V
High-level output current, I_{OH}	-400			-400			μA
Low-level output current, I_{OL}	16			16			mA
Operating free-air temperature, T_A	-55			125			°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT	
V_{IT+}	Positive-going input threshold voltage					200	mV	
V_{IT-}	Negative-going input threshold voltage					-200§	mV	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					120	mV	
V_{IK}	Enable-input clamp voltage	$V_{CC} = \text{MIN}$,	$I_I = -18 \text{ mA}$			-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, See Figure 1	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -400 \text{ μA}$	2.5	3.6		V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{ID} = -200 \text{ mV}$, See Figure 1	$I_{OL} = 8 \text{ mA}$			0.45	V	
			$I_{OL} = 16 \text{ mA}$			0.5		
I_{OZ}	High-impedance-state output current	$V_{CC} = \text{MAX}$, $V_O = 2.7 \text{ V}$	$V_{IL} = 0.8 \text{ V}$, $V_{ID} = -3 \text{ V}$			20	μA	
			$V_{IL} = 0.8 \text{ V}$, $V_{ID} = 3 \text{ V}$			-20		
I_I	Line input current	Other input at 0 V, See Note 3	$V_{CC} = \text{MIN}$, $V_I = 15 \text{ V}$	0.7	1.2	mA		
			$V_{CC} = \text{MAX}$, $V_I = -15 \text{ V}$	-1	-1.7			
I_{IH}	High-level enable-input current	$V_{CC} = \text{MAX}$	$V_{IH} = 2.7 \text{ V}$			20	μA	
			$V_{IH} = 5.25 \text{ V}$			100		
I_{IL}	Low-level enable-input current	$V_{CC} = \text{MAX}$,	$V_{IL} = 0.4 \text{ V}$			-100	μA	
r_i	Input resistance			12	18		kΩ	
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$, See Note 4	$V_{ID} = 3 \text{ V}$, $V_O = 0$	-15	-78	-130	mA	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$,	Outputs disabled			22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.

4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = 0\text{ to }3\text{ V}$, See Figure 2		15	22	ns
t_{PHL} Propagation delay time, high- to low-level output			15	22	ns
t_{PZH} Output enable time to high level	See Figure 3		13	25	ns
t_{PZL} Output enable time to low level			10	25	
t_{PHZ} Output disable time from high level	See Figure 3		19	25	ns
t_{PLZ} Output disable time from low level			17	22	

PARAMETER MEASUREMENT INFORMATION

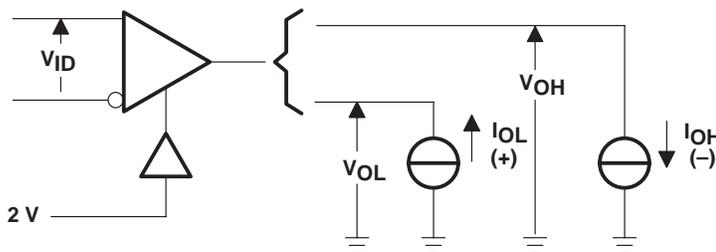
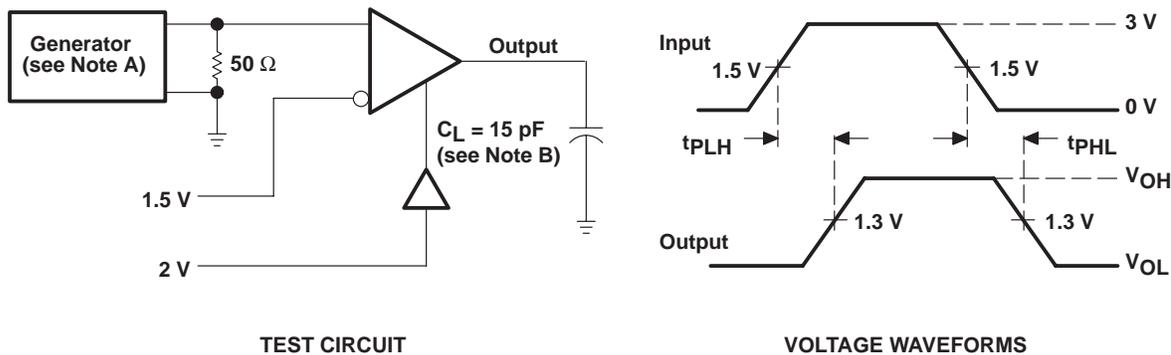


Figure 1. V_{OH} , V_{OL}



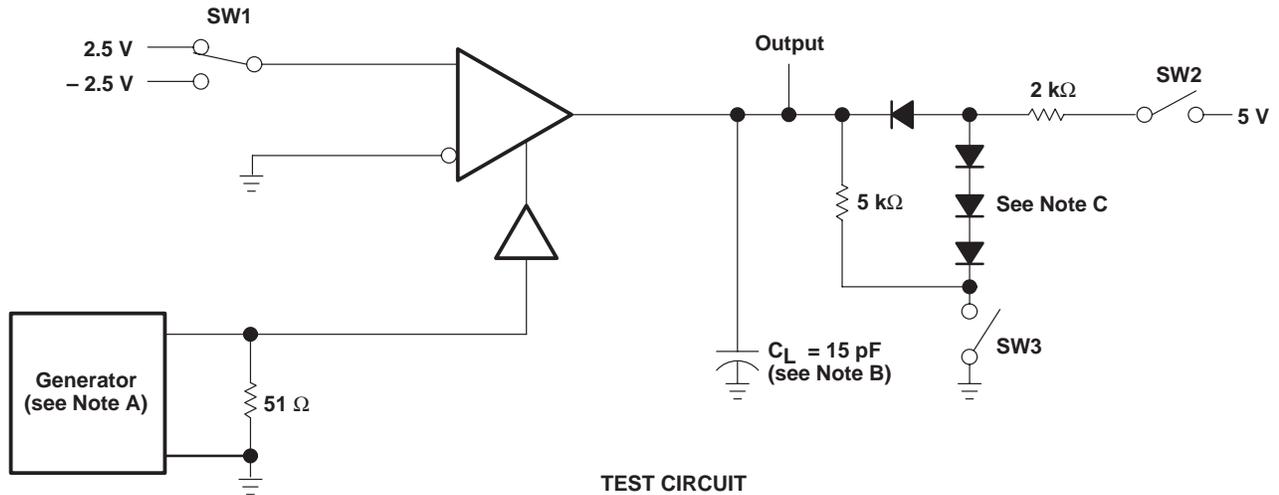
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

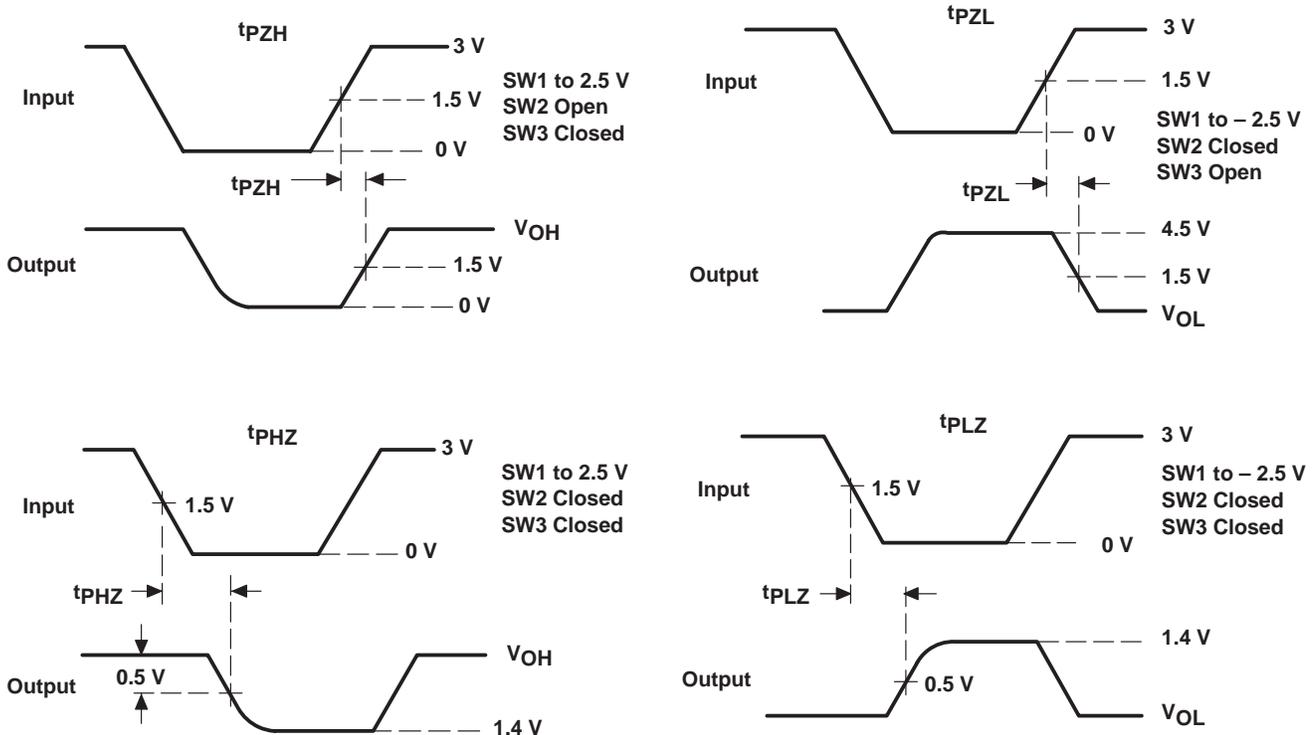
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_O = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

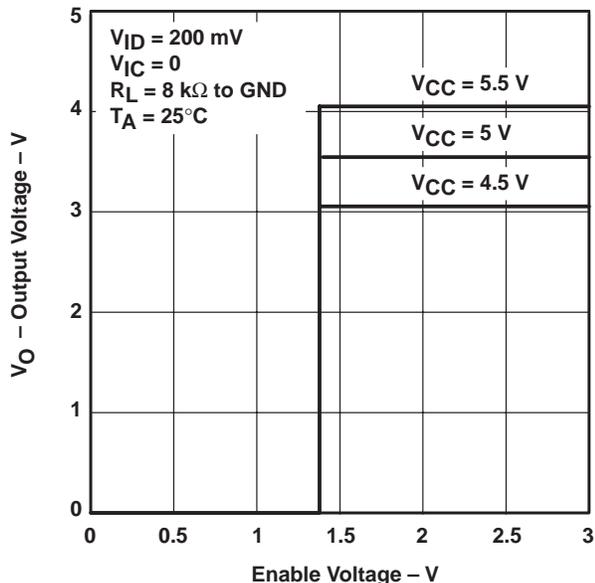


Figure 4

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

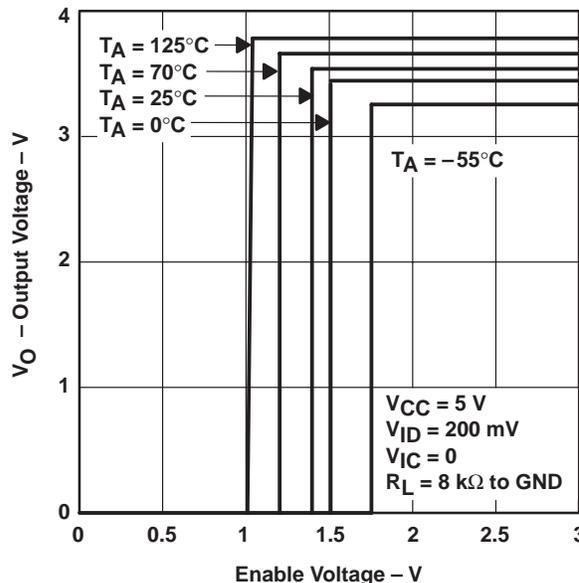


Figure 5

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

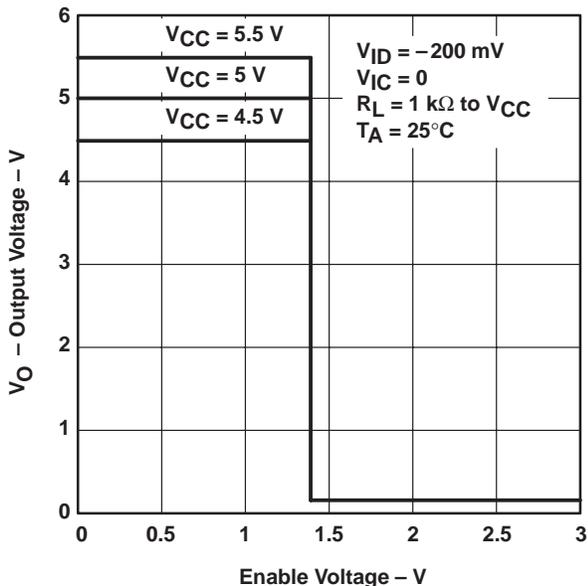


Figure 6

OUTPUT VOLTAGE
 vs
 ENABLE VOLTAGE

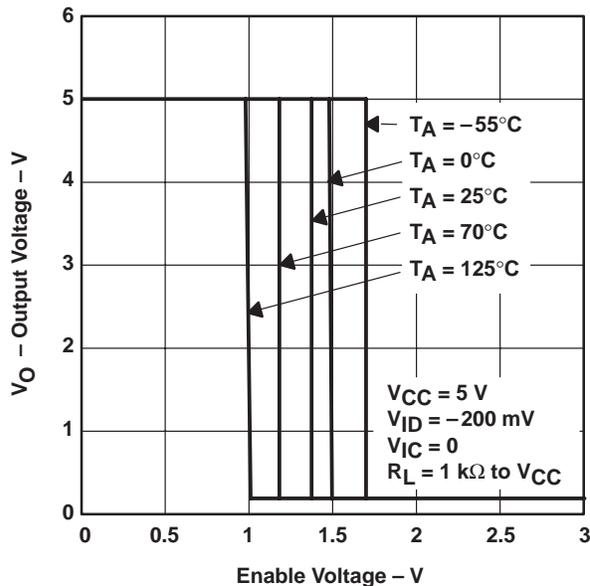


Figure 7

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

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TYPICAL CHARACTERISTICS†

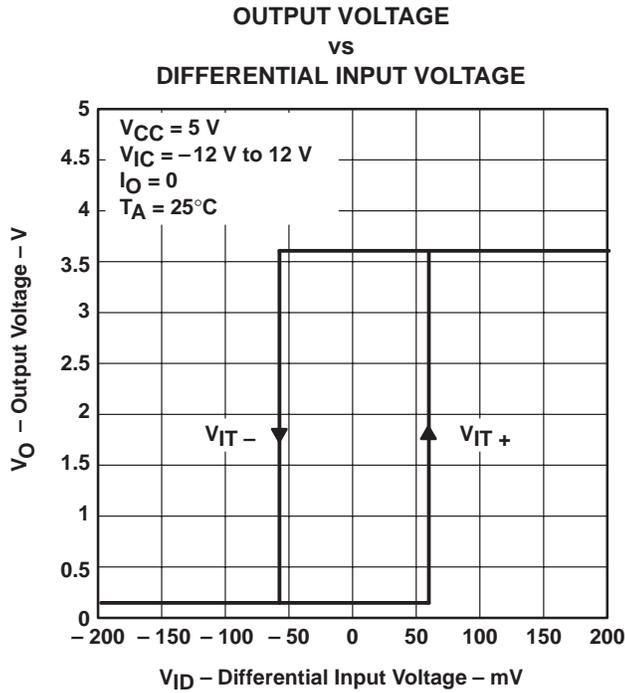


Figure 8

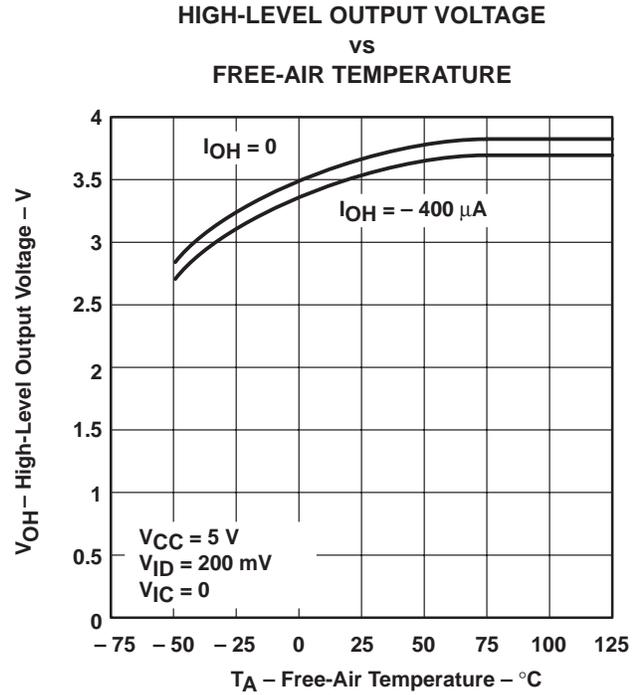


Figure 9

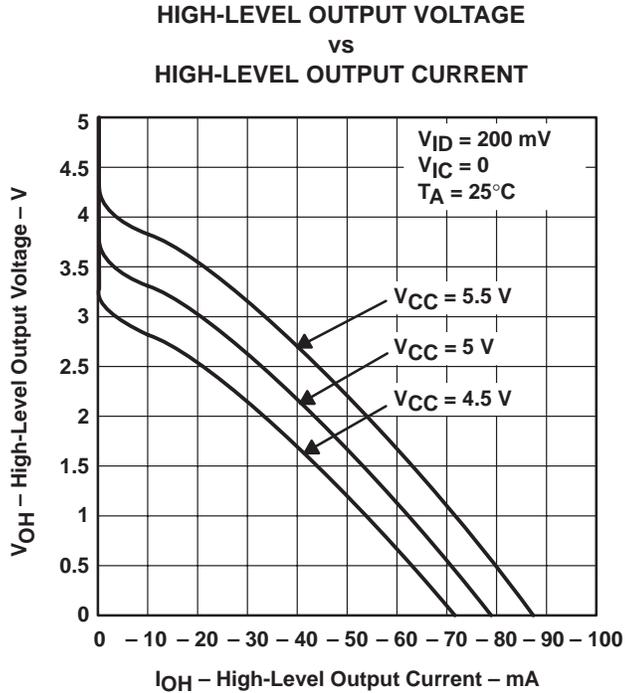


Figure 10

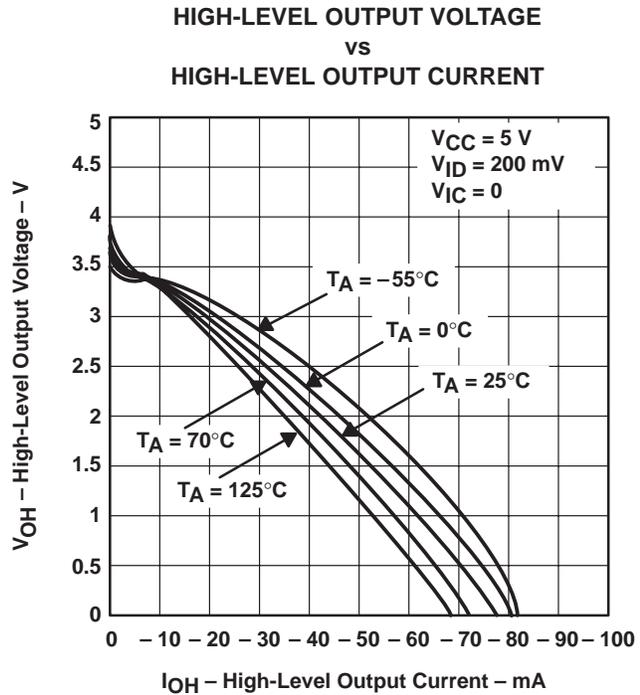


Figure 11

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
 vs
 FREE-AIR TEMPERATURE

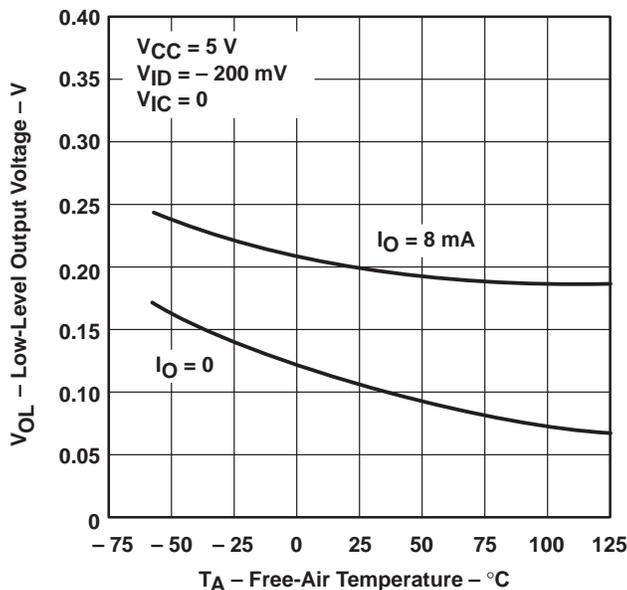


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

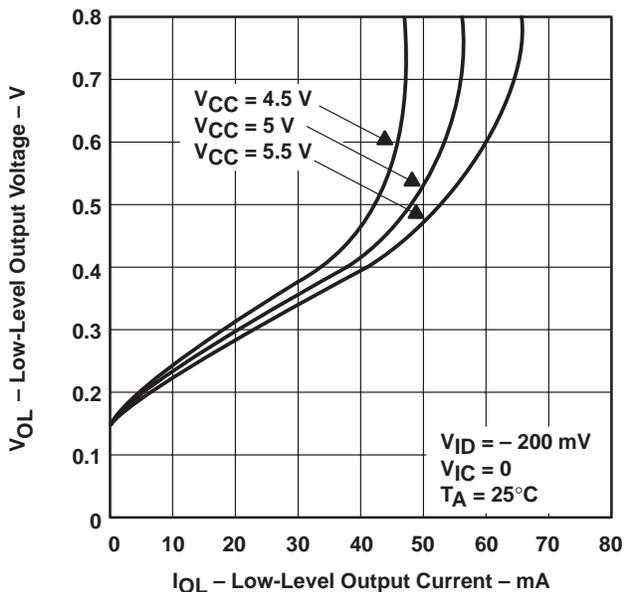


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT

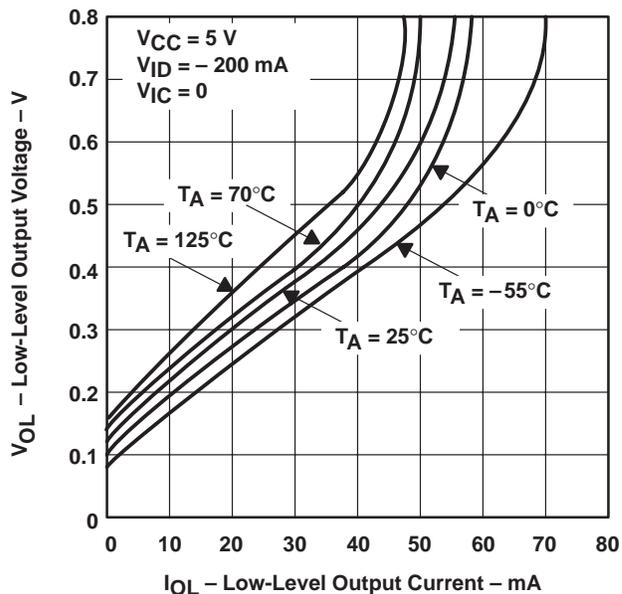


Figure 14

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

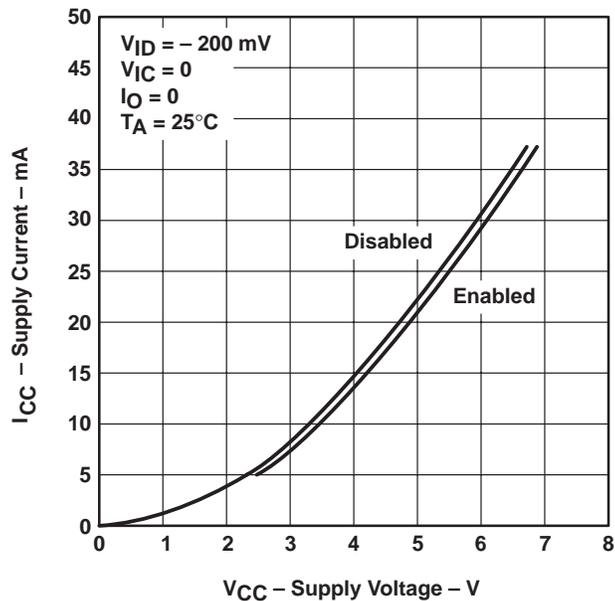


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

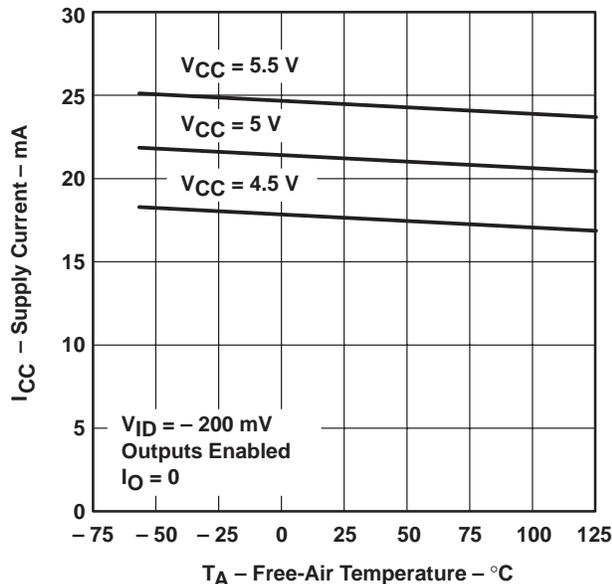


Figure 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

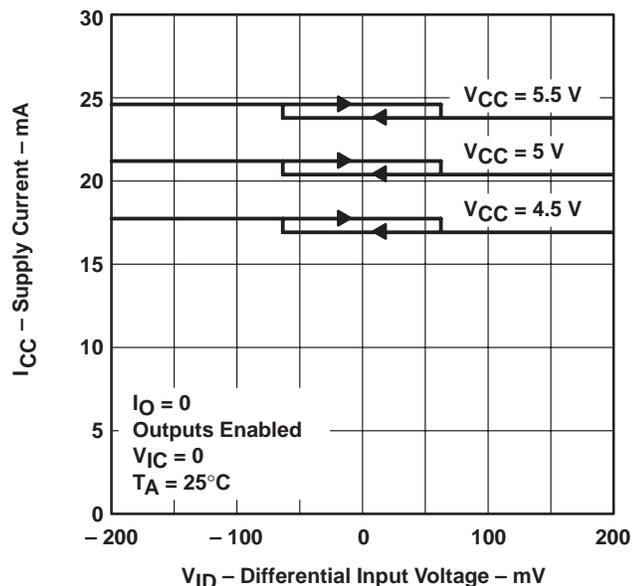


Figure 17

SUPPLY CURRENT
vs
FREQUENCY

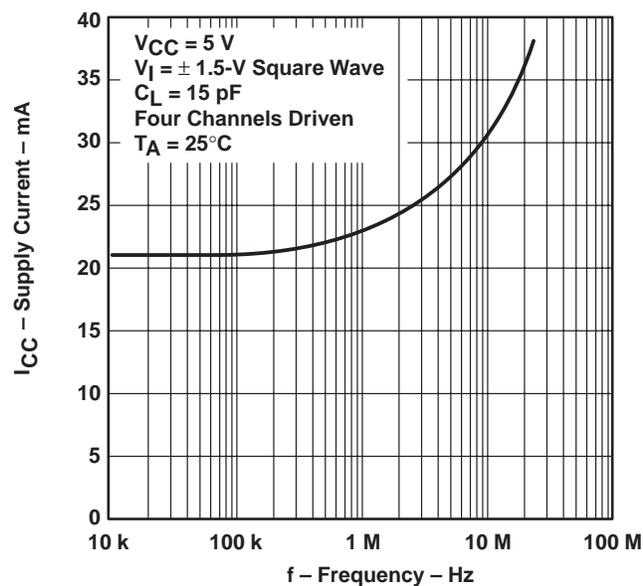


Figure 18

† Data for temperatures below 0°C and above 70°C , and below 4.75 V and above 5.25 V , are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

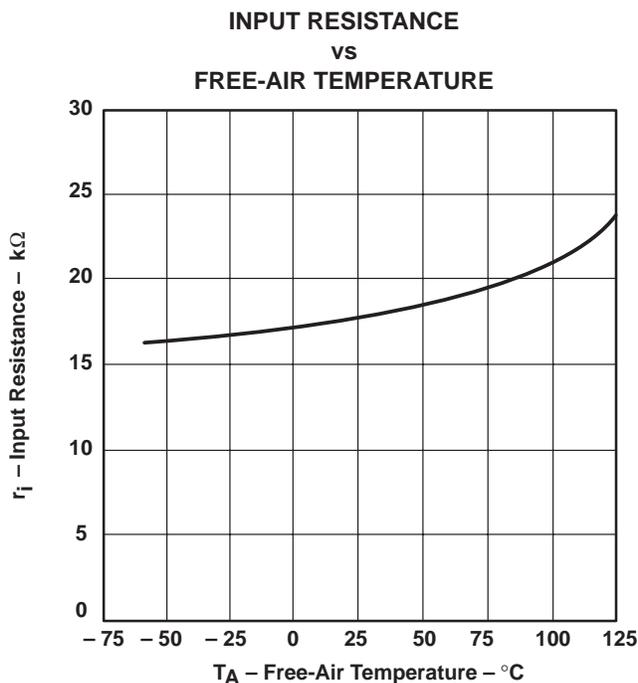


Figure 19

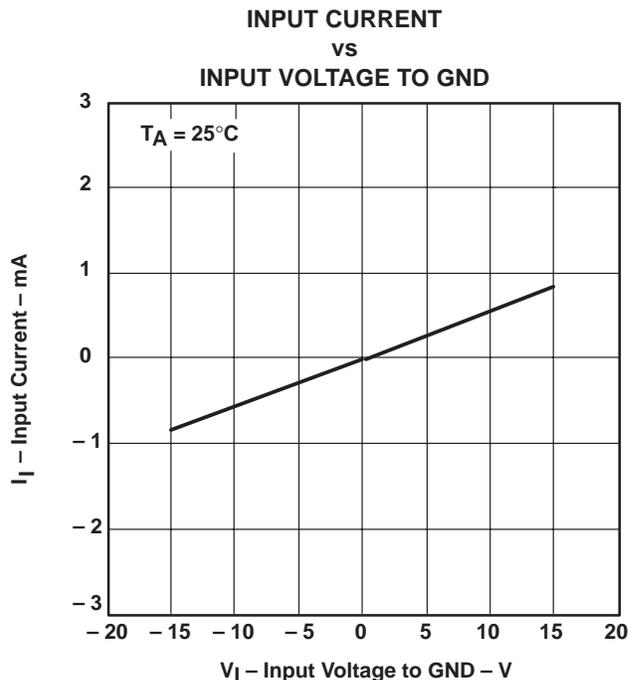


Figure 20

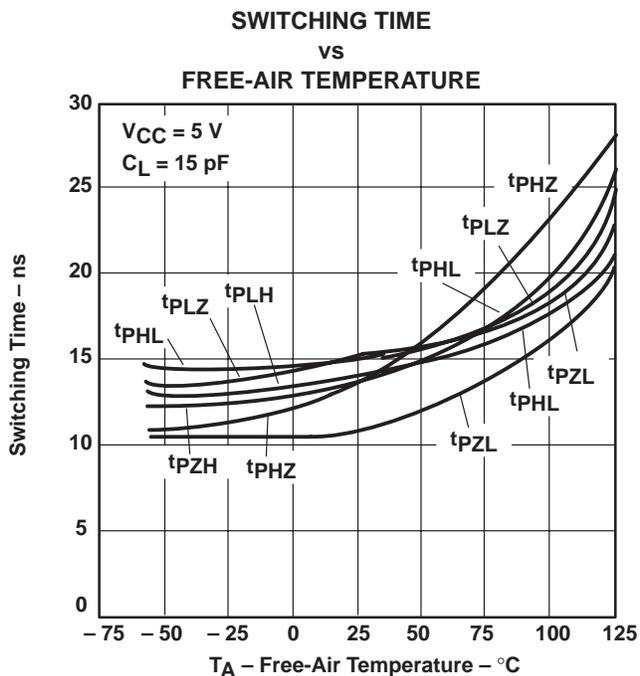


Figure 21

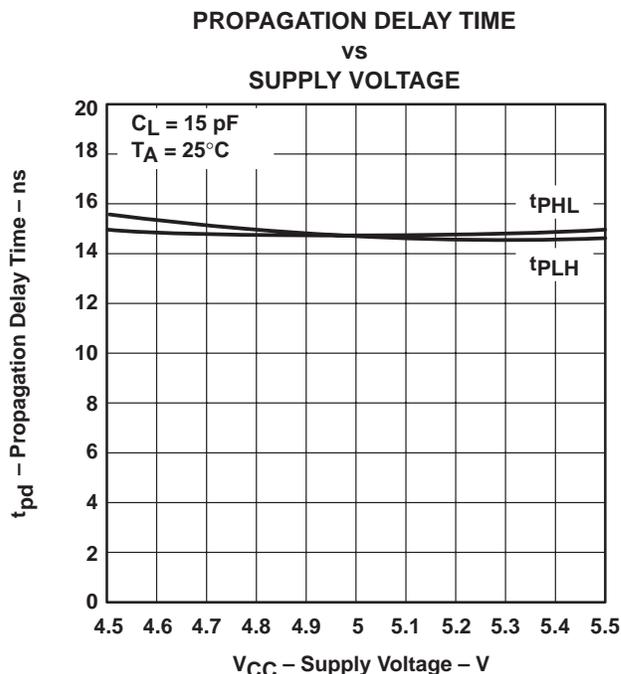


Figure 22

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN55ALS195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75ALS195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN75ALS195N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS195NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ55ALS195FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ55ALS195J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ55ALS195W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

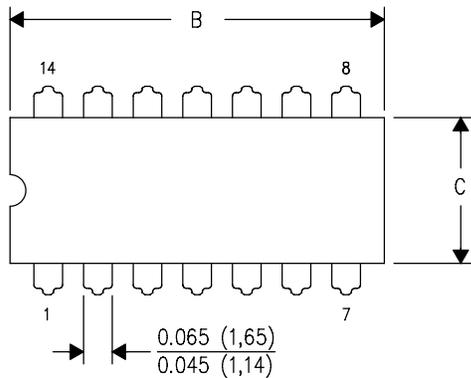
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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

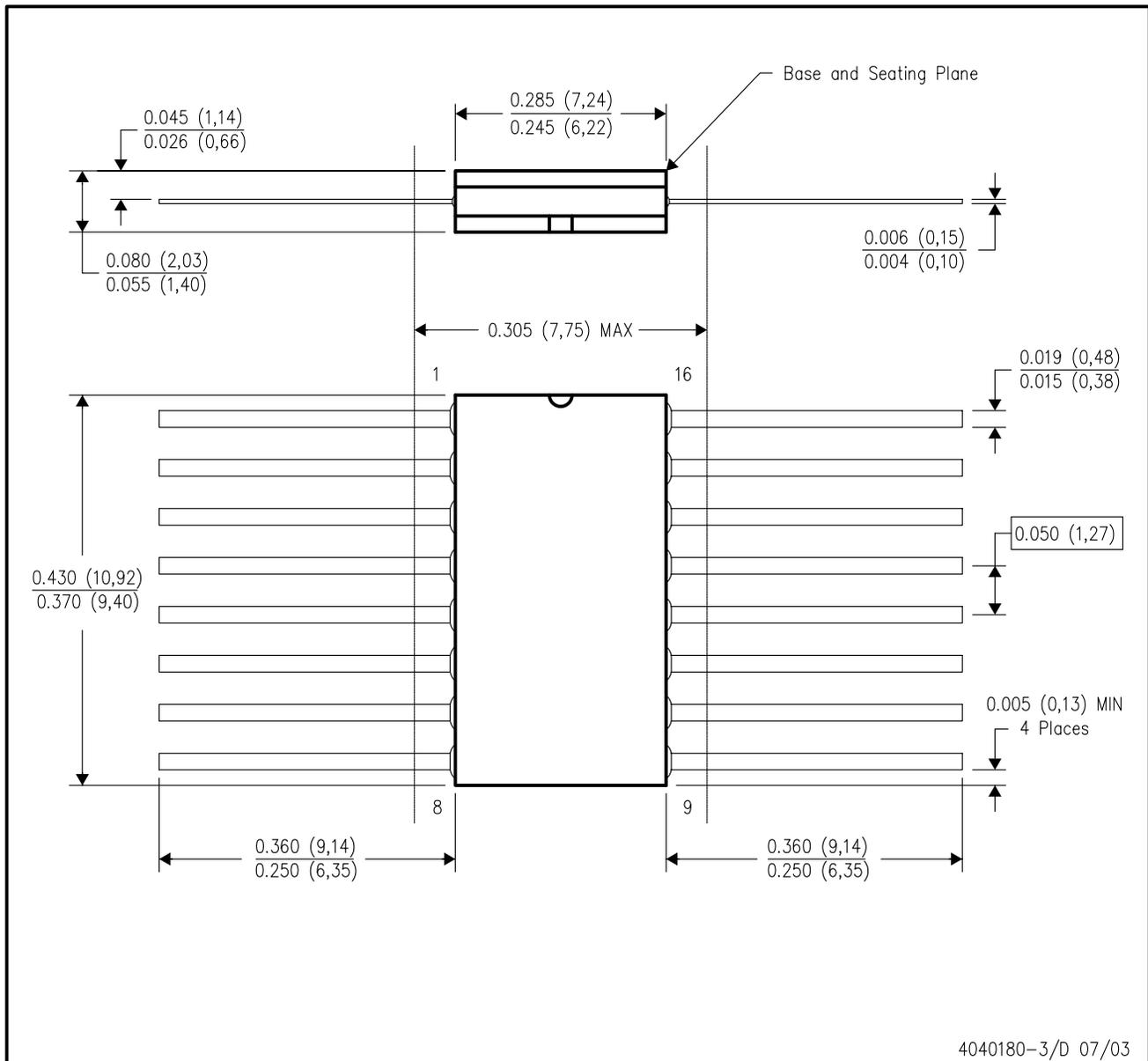


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

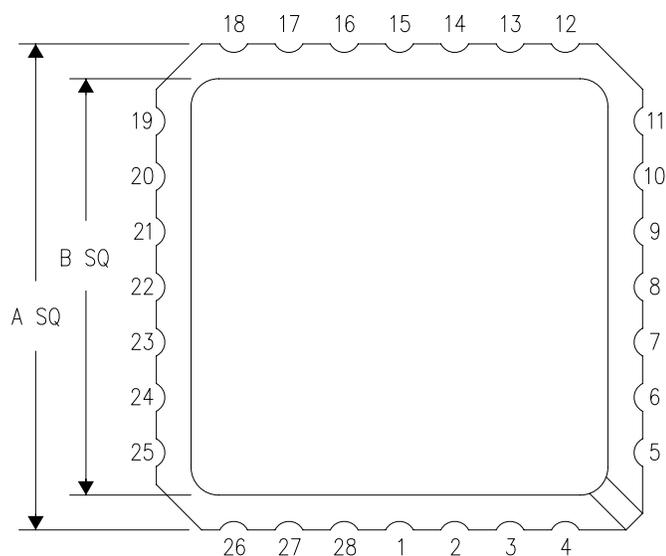


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

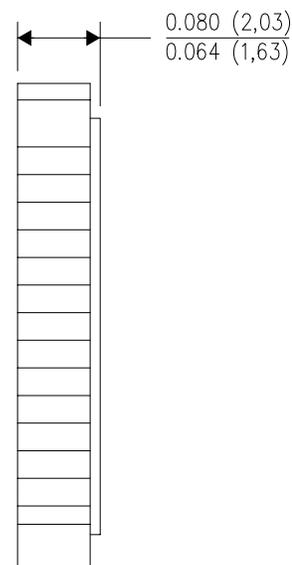
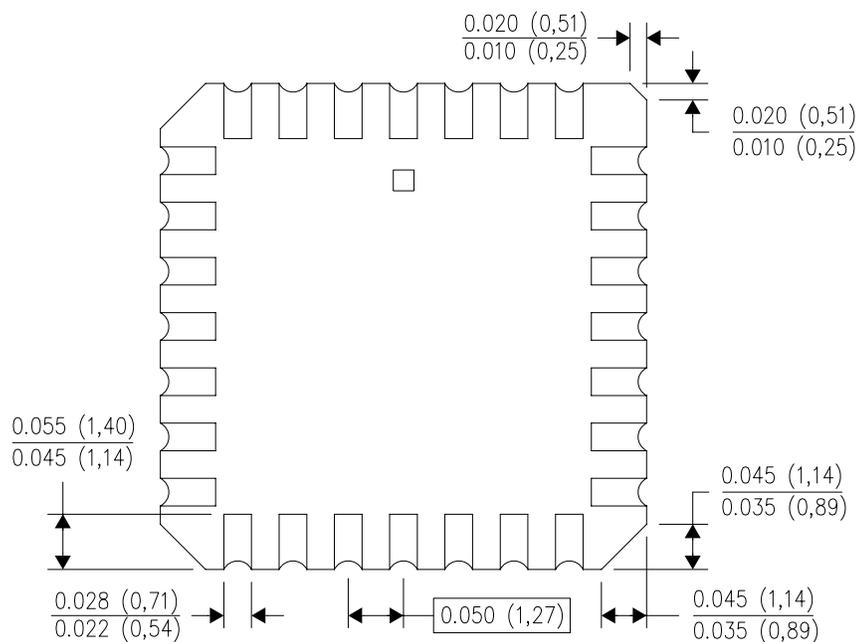
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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