6.0 Gbps SATA PC Board and Cable Equalizer

Check for Samples: SN75LVCP600DRF

FEATURES

- Multirate Operation, 1.5/3.0/6.0 Gbps
- Suitable to Receive 6.0 Gbps Data Over up to 40 Inches (1.0 meter) of FR4 PC Board
- Compensates up to 14dB Loss on the Receive Side and 1.2dB Loss on the Transmit Side at 3 GHz
- Integrated Output Squelch
- Auto Low Power Feature Lowers Power by >80% When Link is in Partial or Slumber Mode
  - <100 mW (Active Mode, typ)
  - <11 mW (Auto Low Power Mode, typ)
- Single 3.3 V Supply
- High Protection Against ESD Transient
  - HBM: 6,000 V
  - CDM: 1,500 V
- Ultra Small Footprint, 2x2 QFN Package

APPLICATIONS

- Notebooks, Desktops, Docking Stations, Servers, Workstations

DESCRIPTION

The SN75LVCP600 is a versatile single channel, SATA signal conditioner supporting data rates up to 6.0Gbps. The device complies with SATA physical link 2m and 3i specifications. The SN75LVCP600 operates from a single 3.3V supply and has 100-Ω line termination with self-biasing feature, making the device suitable for AC coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output when input differential voltage falls below theshold while maintaining a stable common-mode voltage compliant to SATA link. The device is also designed to handle spread spectrum clocking (SSC) transmission per SATA spec.

The SN75LVCP600 handles interconnect losses at its input with selectable equalization settings that can be programmed to match the loss in the channel. For data rates of 3Gbps and lower the LVCP600 equalizes signals for a span of up to 50 inches of FR4 board material. For data rates of 6Gbps the device compensates up to 40in of FR4 material. The equalization level is controlled by the setting of the signal control pin EQ.

Two de-emphasis levels can be selected on the transmit side to provide 0 or 1.2dB of additional high-frequency loss compensation at the output.

The device is hot-plug capable(1) preventing device damage under device *hot*-insertion such as async signal plug/removal, unpowered plug/removal, powered plug/removal, or surprise plug/removal.

(1) Requires use of AC coupling capacitors at differential inputs and outputs.

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75LVCP600DRFR	600	8-Pin DRF reel (large)
SN75LVCP600DRFT	600	8-Pin DRF reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

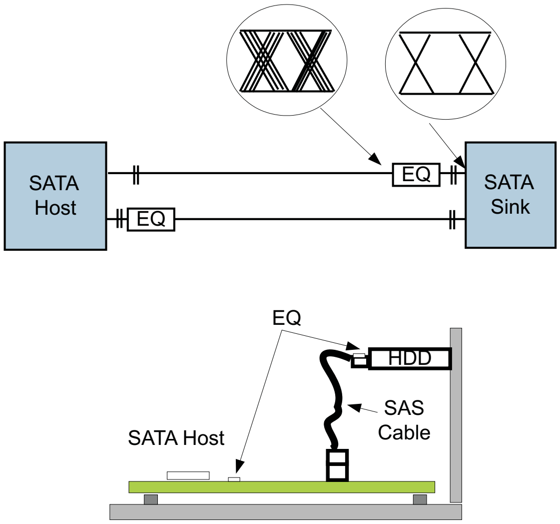


Figure 1. Typical Application

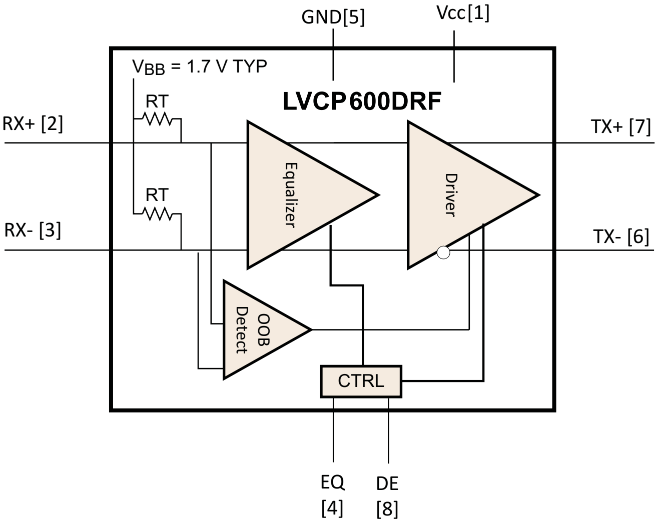
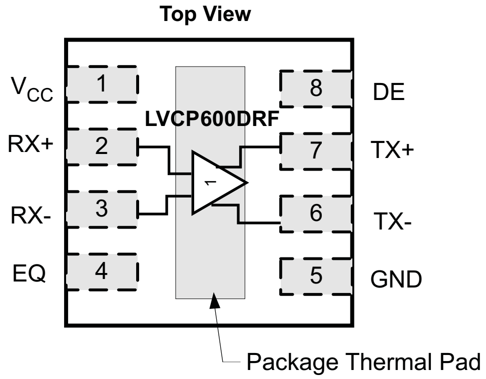


Figure 2. Data Flow Block Diagram

PIN ASSIGNMENTS

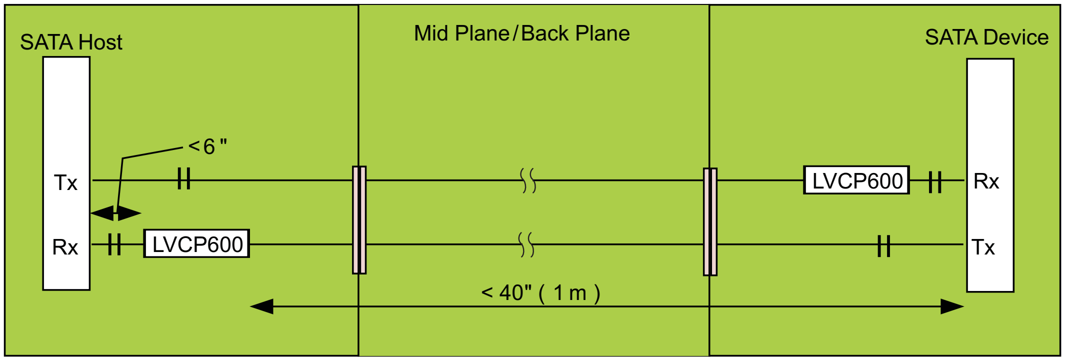


PIN FUNCTIONS

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O			
2	RX+	I, VML	Non-inverting and inverting VML differential inputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
3	RX–	I, VML	
7	TX+	I, VML	Non-inverting and inverting VML differential outputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
6	TX–	I, VML	
CONTROL PINS			
4	EQ	I, LVCMOS	Selects equalization settings per Table 1. Internally tied to GND.
8	DE	I, LVCMOS	Selects de-emphasis settings per Table 1. Internally tied to GND.
POWER			
1	V_{CC}	Power	Positive supply should be 3.3 V ±10%
5	GND	Power	Supply ground

Table 1. EQ and DE Settings

EQ	EQUALIZATION dB (at 6 Gbps)	DE	DE-EMPHASIS dB (at 6 Gbps)
0 (***default***)	7	0 (***default***)	0
1	14	1	–1.2

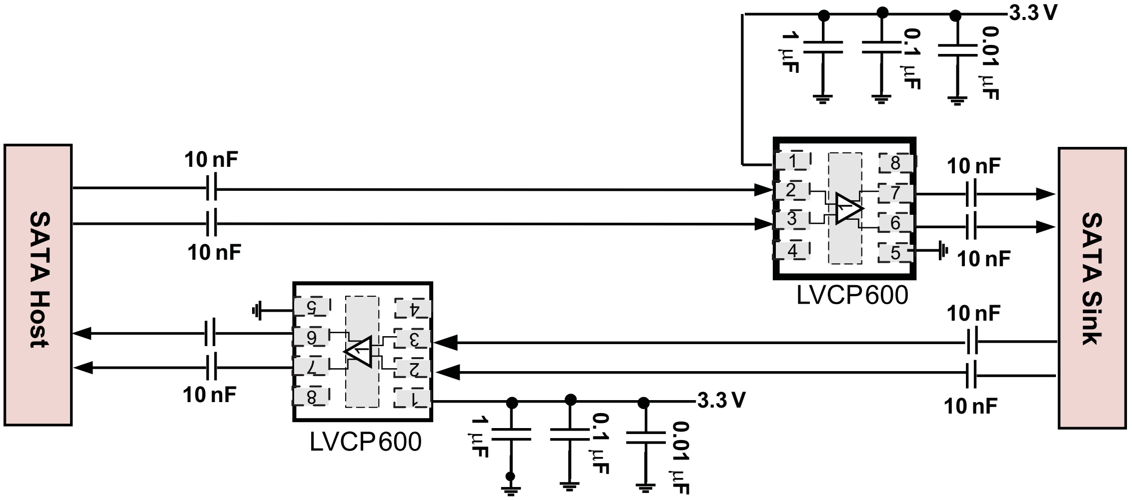


Note:

Trace lengths are suggested values based on TI HSPICE simulations (done over programmable limits of input EQ) to meet SATA loss and jitter spec.

Actual trace length supported by the LVCP600 may be more or less than suggested values and will depend on board layout, trace widths and number of connectors used in the high speed signal path.

Figure 3. Trace Length Example



Note:

1) Place supply caps close to device pin
2) EQ and DE selection at 7 dB and 0dB respectively
3) Actual EQ /DE settings will depend on device placement relative to host and SATA connector

Figure 4. Typical Device Implementation

The LVCP600 allows user to take the guess work of using a signal conditioning device in a SATA link. With the LVCP600 user has the option to use or remove the device based on signal conditioning needs. See Figure 5.

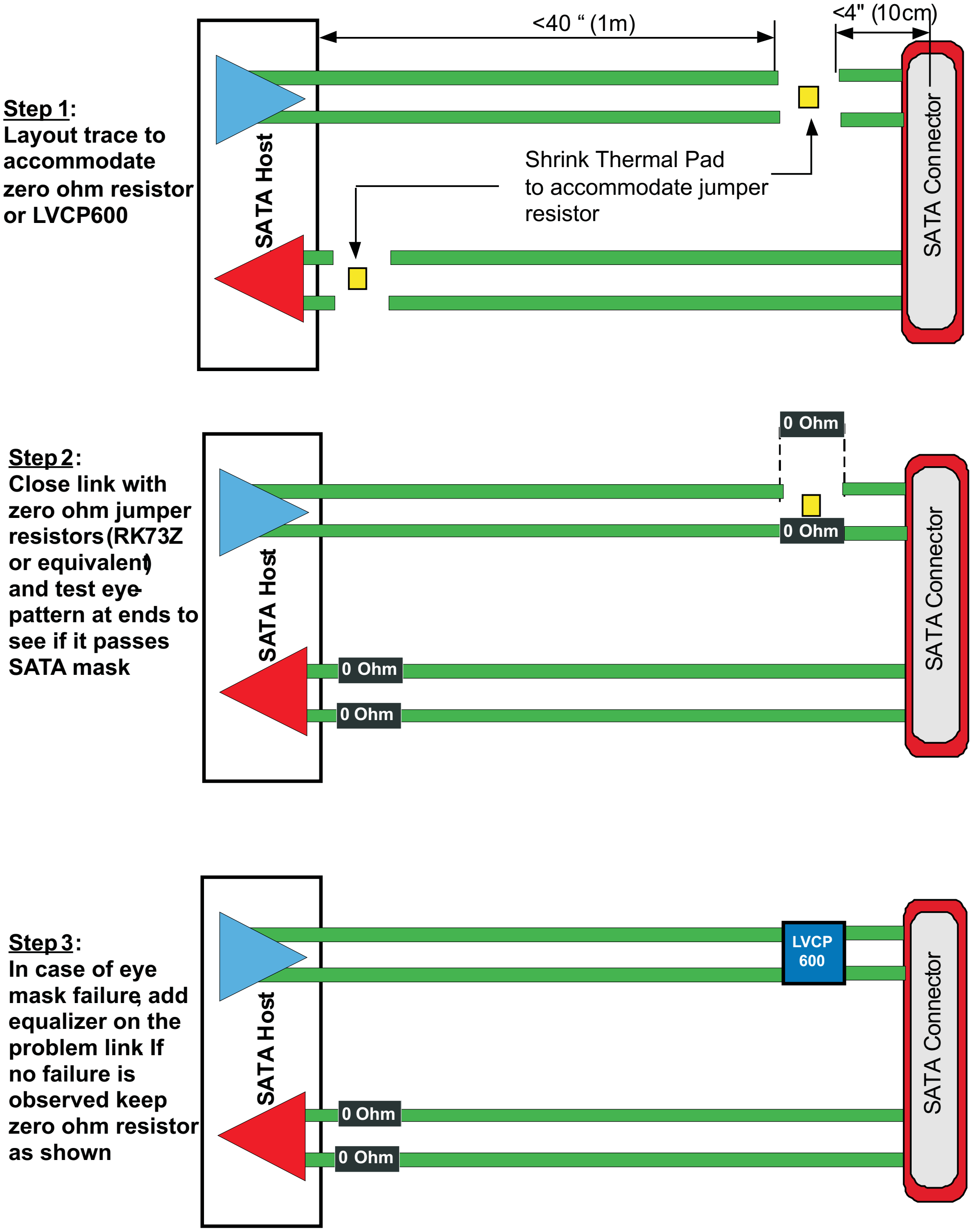


Figure 5. Implementation Guideline

OPERATION DESCRIPTION

INPUT EQUALIZATION

The SN75LVCP600 supports programmable equalization in its front stage; the equalization settings are shown in Table 1. The input equalizer is designed to recover a signal even when no eye is present at the receiver and will affectively support FR4 trace at the input anywhere from 4" to 40" at SATA 6G speed.

AUTO LOW POWER (ALP) MODE (see Figure 10)

Auto Low Power (ALP) Mode is triggered when a channel is in the electrical idle state for >10 µs.

- The device enters and exits Low Power Mode by actively monitoring input signal (VID_{pp}) level. When the input signal is in the electrical idle state, i.e., VID_{pp} <50 mV and stays in this state for >10 µs, the device automatically enters the low power state. In this state the output is driven to VCM and the device selectively shuts off internal circuitry to lower power by >90% of its normal operating power. While in ALP mode the device continues actively to monitor input signal levels. When the input signal exceeds the SATA OOB upper threshold level, the device reverts to the active state. Exit time from Auto Low Power Mode is <50 ns (max).

OUT-OF-BAND (OOB) SUPPORT

The squelch detector circuit within the device enables full detection of OOB signaling as specified in the SATA spec. When differential signal amplitude at the receiver input is 50 mV_{pp} or less, the output is squelched. Differential signal amplitude of 90 mV_{pp} or more is detected as an activity and therefore passed to the output indicating activity. Squelch circuit ON/OFF time is 5 ns max. While in squelch mode outputs are held to VCM.

DEVICE POWER

The SN75LVCP600 is designed to operate from a single 3.3 V supply. Always practice proper power supply sequencing procedure. Apply V_{CC} first before any input signals are applied to the device. The power down sequence is in reverse order.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 4	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to V_{CC} + 0.5	V
Electrostatic discharge	Human body model(3)	±6000	V
	Charged-device model(4)	±1500	V
	Machine model(5)	±200	V
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

THERMAL INFORMATION

THERMAL METRIC(1)		SN75LVCP600	UNITS
		DRF (8) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	97.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	81.9	
θ_{JB}	Junction-to-board thermal resistance	65.6	
ψ_{JT}	Junction-to-top characterization parameter	1.3	
ψ_{JB}	Junction-to-board characterization parameter	65.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	19.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C; all temperature limits are specified by design

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	Coupling capacitor			12		nF
T_A	Operating free-air temperature		0		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
ICC_{Max}	Active mode supply current	EQ/DE = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mV_{pp}		29	40	mA
I_{CCPS}	Auto power save mode I_{CC}	When auto low power conditions are met		3.3	5.9	mA
	Maximum data rate				6.0	Gbps
t_{PDelay}	Propagation delay	Measured using K28.5 pattern, See Figure 8		275	350	ps
$AutoLP_{ENTRY}$	Auto low power entry time	Electrical idle at input, See Figure 10		11		µs
$AutoLP_{EXIT}$	Auto low power exit time	After first signal activity, See Figure 10		33	50	ns
OOB						
V_{OOB}	Input OOB threshold	F = 750 MHz	50	70	90	mV_{pp}
$D_{VdiffOOB}$	OOB differential delta				25	mV
D_{VCMOOB}	OOB common-mode delta				50	mV
t_{OOB1}	OOB mode enter	See Figure 9		1	5	ns
t_{OOB2}	OOB mode exit	See Figure 9		1	5	ns
CONTROL LOGIC						
V_{IH}	High-level input voltage	For all control pins	1.4			V
V_{IL}	Low-level input voltage				0.5	V
VIN_{HYS}	Input hysteresis			115		mV
I_{IH}	High-level input current	$V_{IH} = V_{CC}$ (DE/EQ)			20	µA
I_{IL}	Low-level input current	V_{IL} = 0V (DE/EQ)			10	µA
RECEIVER AC/DC						
Z_{DIFFRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.7		V
RL_{DiffRX}	Differential mode return loss (RL)	f = 150 MHz–300 MHz	18	26		dB
		f = 300 MHz–600 MHz	14	22		
		f = 600 MHz–1.2 GHz	10	17		
		f = 1.2 GHz–2.4 GHz	8	12		
		f = 2.4 GHz–3.0 GHz	3	11		
$RX_{DiffRLSlope}$	Differential mode RL slope	f = 300 MHz–6.0 GHz (see Figure 6)		–13		dB/dec
RL_{CMRX}	Common-mode return loss	f = 150 MHz–300 MHz	5	9.4		dB
		f = 300 MHz–600 MHz	5	17		
		f = 600 MHz–1.2 GHz	2	18		
		f = 1.2 GHz–2.4 GHz	1	9.9		
		f = 2.4 GHz–3.0 GHz	1	8.6		
V_{diffRX}	Differential input voltage PP	f = 1.5 GHz and 3.0 GHz	120		1600	mV/ppd

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
IB_{RX}	Impedance balance	f = 150 MHz–300 MHz	30	41		dB
		f = 300 MHz–600 MHz	30	41		
		f = 600 MHz–1.2 GHz	20	34		
		f = 1.2 GHz–2.4 GHz	10	24		
		f = 2.4 GHz–3.0 GHz	10	26		
		f = 3.0 GHz–5.0 GHz	4	18		
		f = 5.0 GHz–6.5 GHz	4	18		
$T_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA 6 Gbps speed measured 1" from device pin	62		75	ps
T_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX– signal falling/rising edge			30	ps
TRANSMITTER AC/DC						
Z_{diffTX}	Pair differential impedance		85	100	122	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
$V_{TXtrans}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2	0.3	1.2	V
RL_{DiffTX}	Differential mode return loss	f = 150 MHz–300 MHz	13	22		dB
		f = 300 MHz–600 MHz	8	21		
		f = 600 MHz–1.2 GHz	6	19		
		f = 1.2 GHz–2.4 GHz	6	14		
		f = 2.4 GHz–3.0 GHz	3	14		
$TX_{DiffRLSlope}$	Differential mode RL slope	f = 300 MHz – 3.0 GHz (see Figure 6)		–13		dB/dec
RL_{CMTX}	Common-mode return loss	f = 150 MHz–300 MHz	5	20		dB
		f = 300 MHz–600 MHz	5	16		
		f = 600 MHz–1.2 GHz	2	13		
		f = 1.2 GHz–2.4 GHz	1	8		
		f = 2.4 GHz–3.0 GHz	1	8		
IB_{TX}	Impedance balance	f = 150 MHz–300 MHz	30	38		dB
		f = 300 MHz–600 MHz	30	38		
		f = 600 MHz–1.2 GHz	20	33		
		f = 1.2 GHz–2.4 GHz	10	25		
		f = 2.4 GHz–3.0 GHz	10	25		
		f = 3.0 GHz–5.0 GHz	4	21		
		f = 5.0 GHz–6.5 GHz	4	21		
$Diff_{VppTX}$	Differential output voltage swing	f = 3.0 GHz (under no interconnect loss)	400	650	900	mV/ppd
VCM_{AC_TX}	TX AC CM voltage	At 1.5 GHz		15	50	mVppd
		At 3.0 GHz		10	26	dBmv (rms)
		At 6.0 GHz		12	30	
VCM_{TX}	Common-mode voltage			1.70		V
$T_{20\text{-}80TX}$	Rise/Fall time	Rise times and fall times measured between 20% and 80% of the signal. At 6Gbps under no load conditions measured at the pin	44	58	85	ps
T_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX– signal falling/rising edge, D1, D0 = V_{CC}		2	20	ps
TxR/F_{Imb}	TX rise/fall imbalance	At 3 Gbps		6%	20%	
$TxAm_{pImb}$	TX amplitude imbalance			1%	10%	

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER JITTER(1)						
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 333 ps, K28.5 control character, See Figure 7		0.12	0.19	UI_{pp}
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 333 ps, K28.7 control character, See Figure 7		1.0	2.0	ps-rms
DJ_{TX}	Residual deterministic jitter	VID = 500 mV_{pp}, UI = 167 ps, K28.5 control character, See Figure 7		0.12	0.34	UI_{pp}
RJ_{TX}	Random jitter	VID = 500 mV_{pp}, UI = 167 ps, K28.7 control character, See Figure 7		0.95	2.0	ps-rms

(1) $T_J = (14.1 \times RJ_{SD} + DJ)$ where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. Jitter measurement is at the SATA connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect as shown in Figure 7.

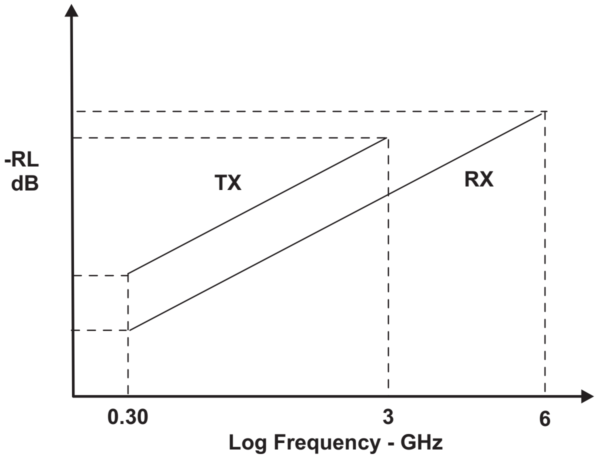


Figure 6. TX, RX Differential Return Loss Limits

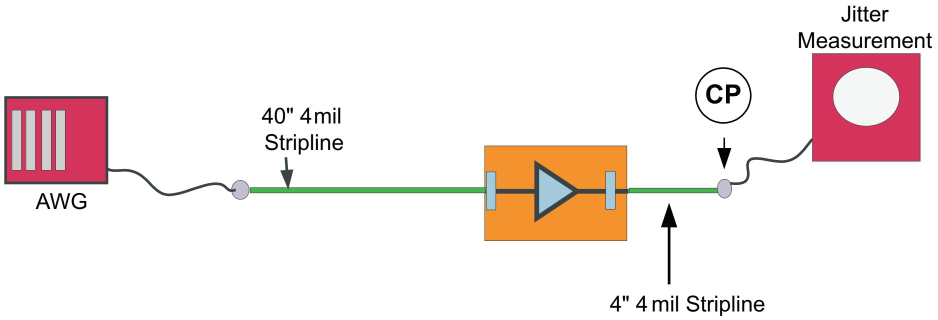


Figure 7. Jitter Measurement Test Condition

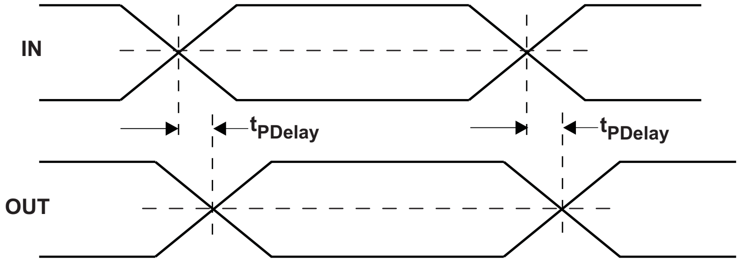


Figure 8. Propagation Delay Timing Diagram

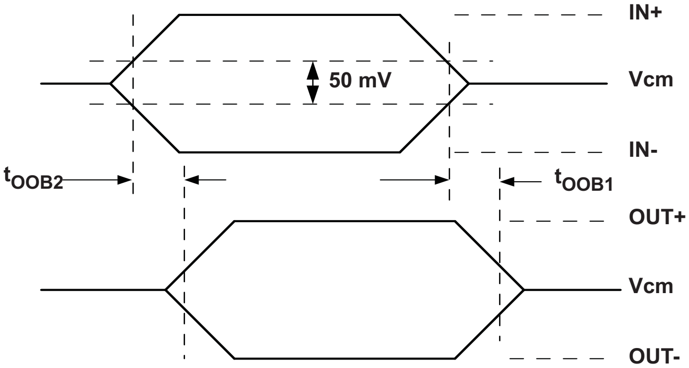


Figure 9. OOB Enter and Exit Timing

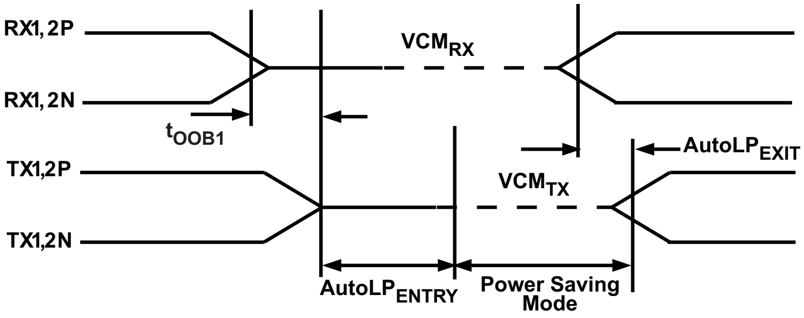


Figure 10. Auto Low Power Mode Entry and Exit Timing

APPLICATION INFORMATION

Figure 12 through Figure 24 show LVCP600 typical performance plots when connected to various trace lengths with V_{CC} = 3.3 V and T_A = 25°C. All eye diagrams measured using K28.5 pattern at 6 Gbps. Setup for the performance plots is shown in Figure 11.

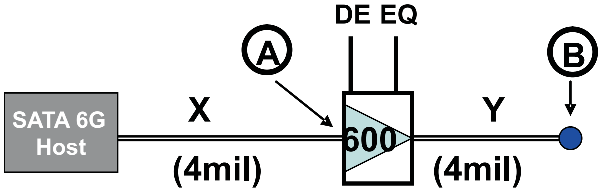
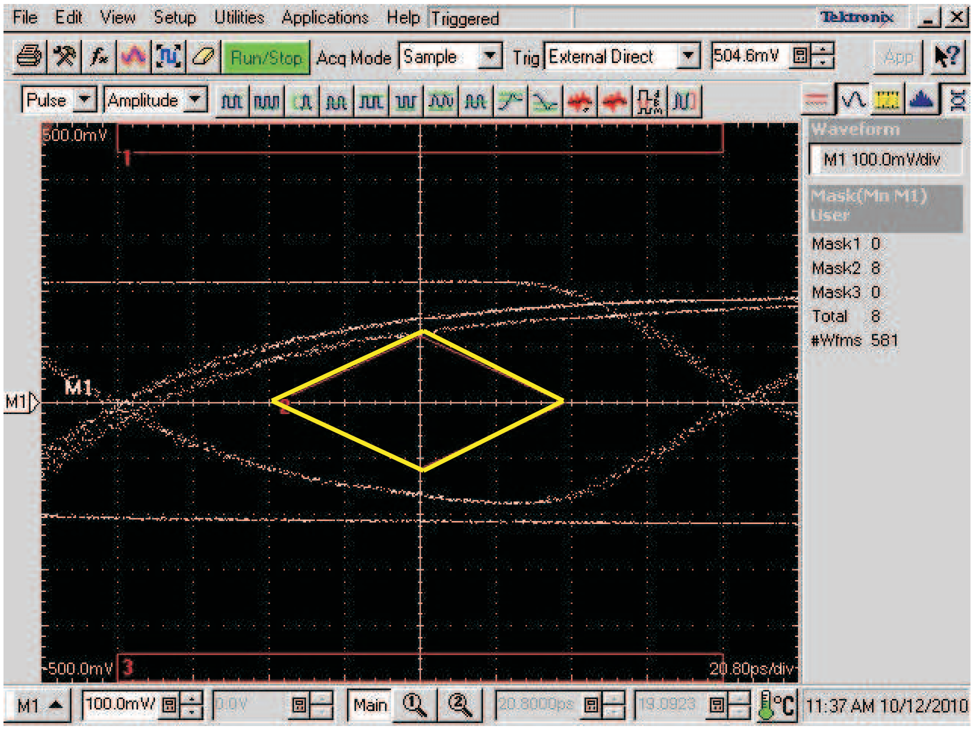


Figure 11. Test Points



Triggered

Acq Mode Sample

Trig External Direct

504.6mV

Waveform

M1 100.0mV/div

Mask(Mn M1)
User

Mask1 0
Mask2 8
Mask3 0
Total 8
#Wfms 581

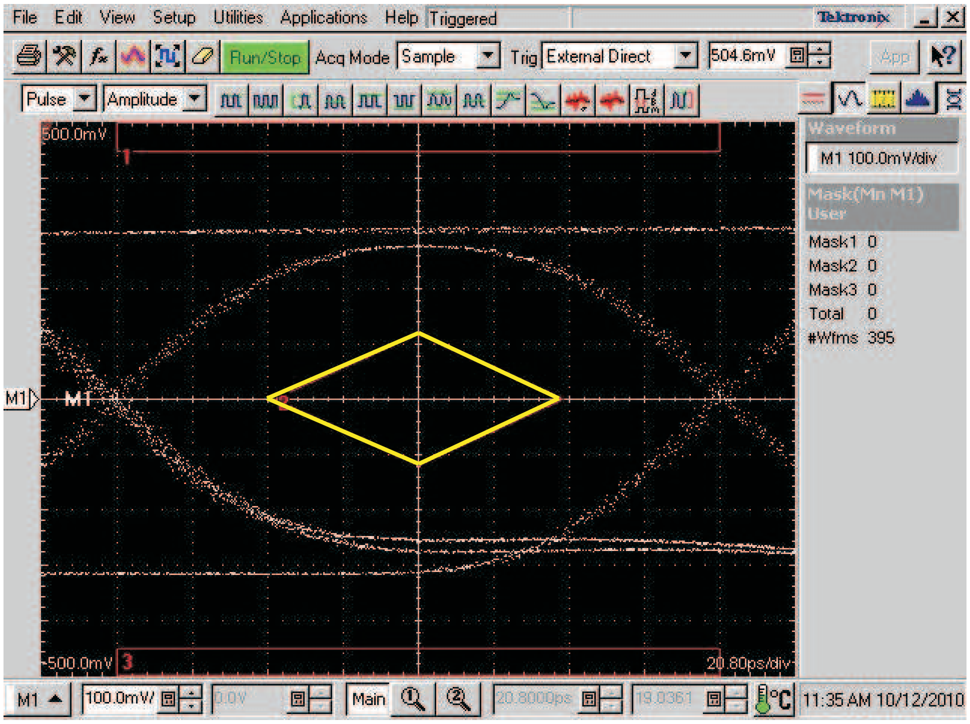
500.0mV

-500.0mV

20.80ps/div

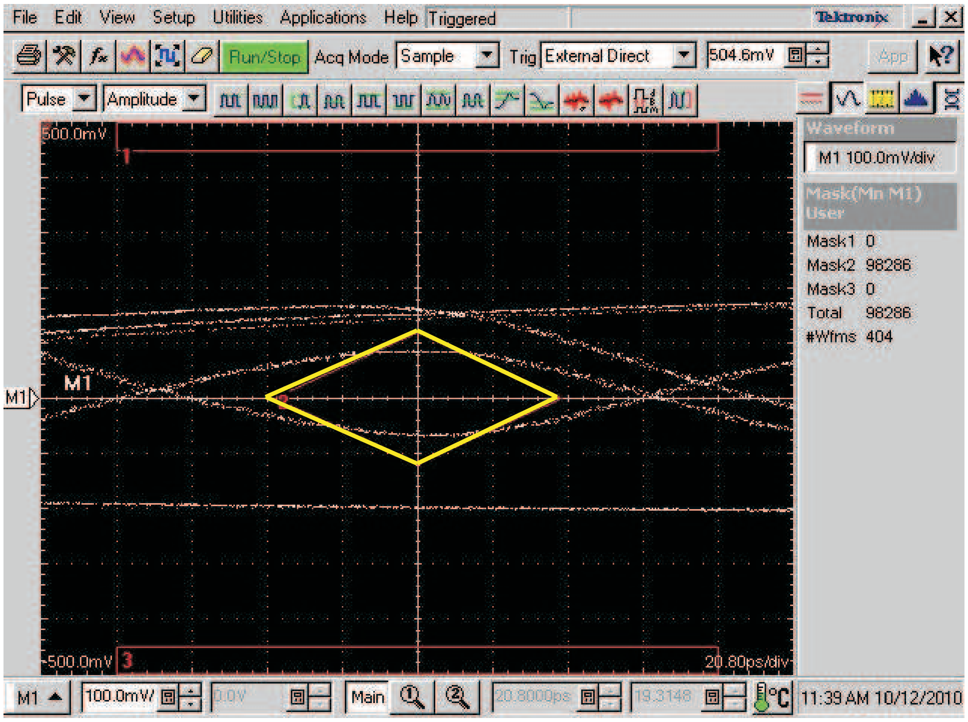
M1 100.0mV 0.0V Main 20.8000ps 19.0923 °C 11:37 AM 10/12/2010

Figure 12. Eye Pattern at A → X= 8”; Y = 2” DE = 1 EQ = 0



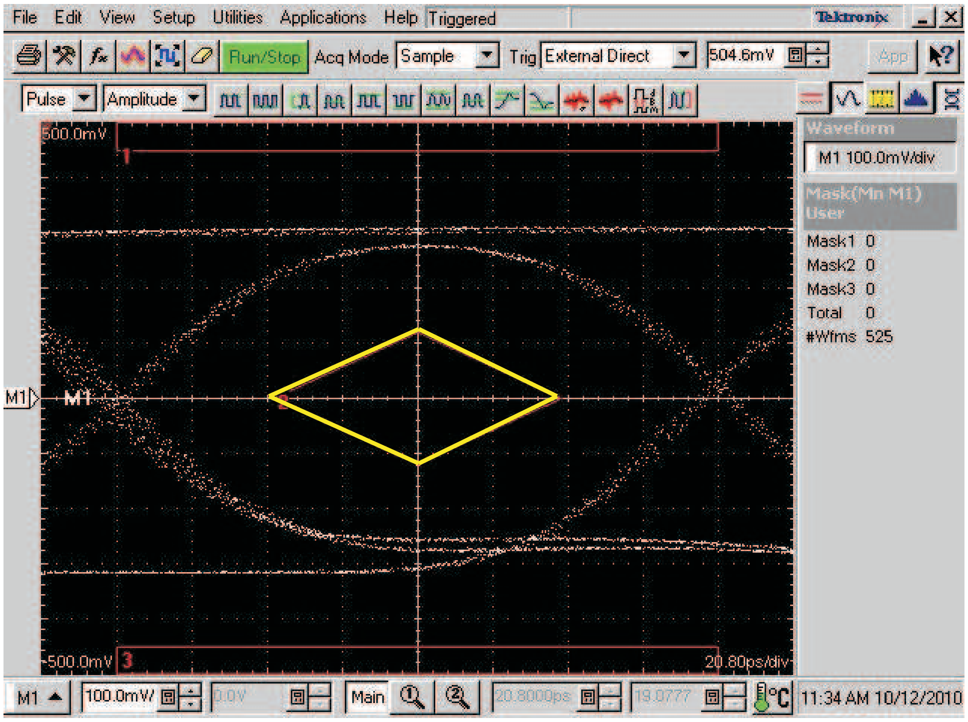
Acq Mode Sample
Trig External Direct
504.6mV
Pulse
Amplitude
M1 100.0mV/div
Mask1 0
Mask2 0
Mask3 0
Total 0
#Wfms 395
500.0mV
-500.0mV
20.80ps/div
M1 100.0mV
0.0V
20.8000ps
19.0361
11:35 AM 10/12/2010

Figure 13. Eye Pattern at B → X= 8”; Y = 2” DE = 1 EQ = 0



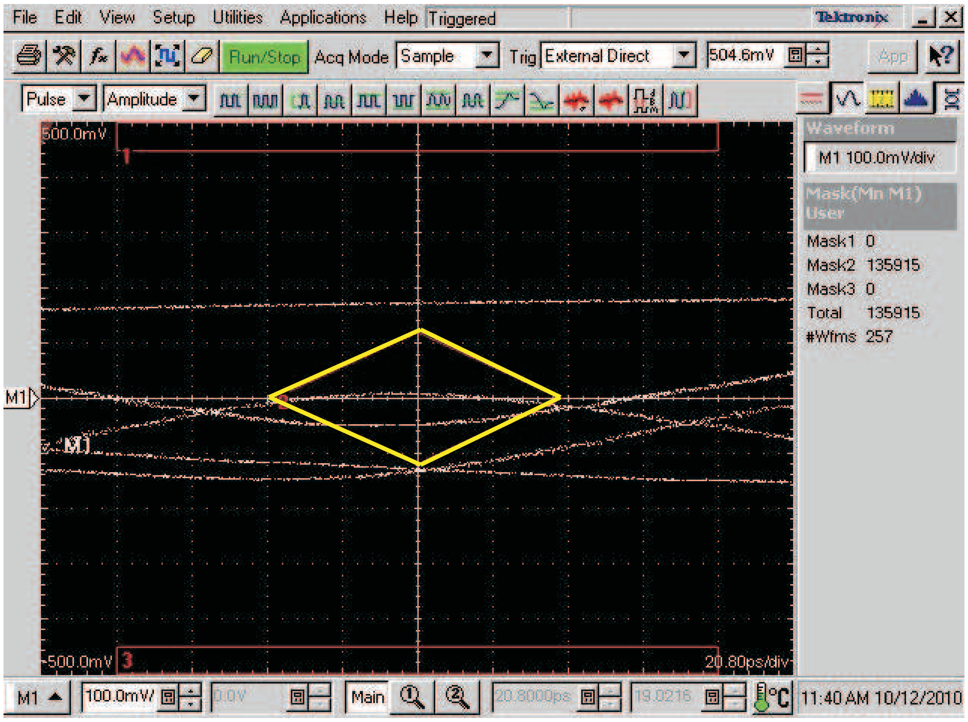
Acq Mode Sample
Trig External Direct
504.6mV
Pulse
Amplitude
M1 100.0mV/div
Mask1 0
Mask2 98286
Mask3 0
Total 98286
#Wfms 404
500.0mV
-500.0mV
20.80ps/div
M1 100.0mV
0.0V
20.8000ps
19.3148
11:39 AM 10/12/2010

Figure 14. Eye Pattern at A → X= 16”; Y = 2” DE = 1 EQ = 0



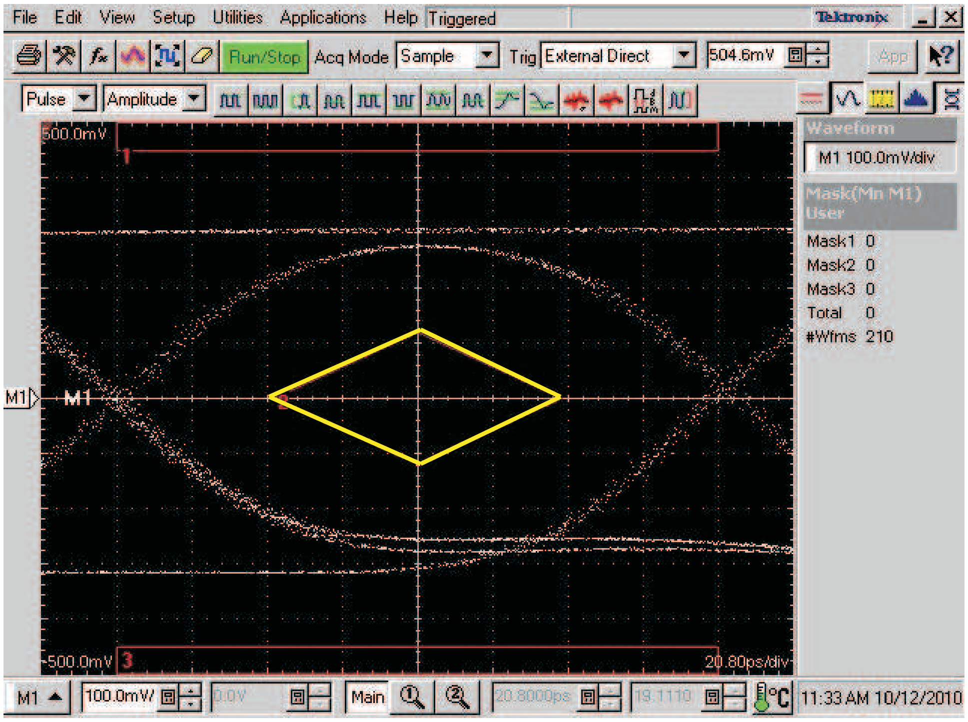
Acq Mode Sample
Trig External Direct
504.6mV
M1 100.0mV/div
Mask1 0
Mask2 0
Mask3 0
Total 0
#Wfms 525
M1 100.0mV 0.0V 20.8000ps 19.0777
11:34 AM 10/12/2010

Figure 15. Eye Pattern at B → X= 16”; Y = 2” DE = 1 EQ = 0



Acq Mode Sample
Trig External Direct
504.6mV
M1 100.0mV/div
Mask1 0
Mask2 135915
Mask3 0
Total 135915
#Wfms 257
M1 100.0mV 0.0V 20.8000ps 19.0216
11:40 AM 10/12/2010

Figure 16. Eye Pattern at A → X= 24”; Y = 2” DE = 1 EQ = 0



Acq Mode Sample

Trig External Direct

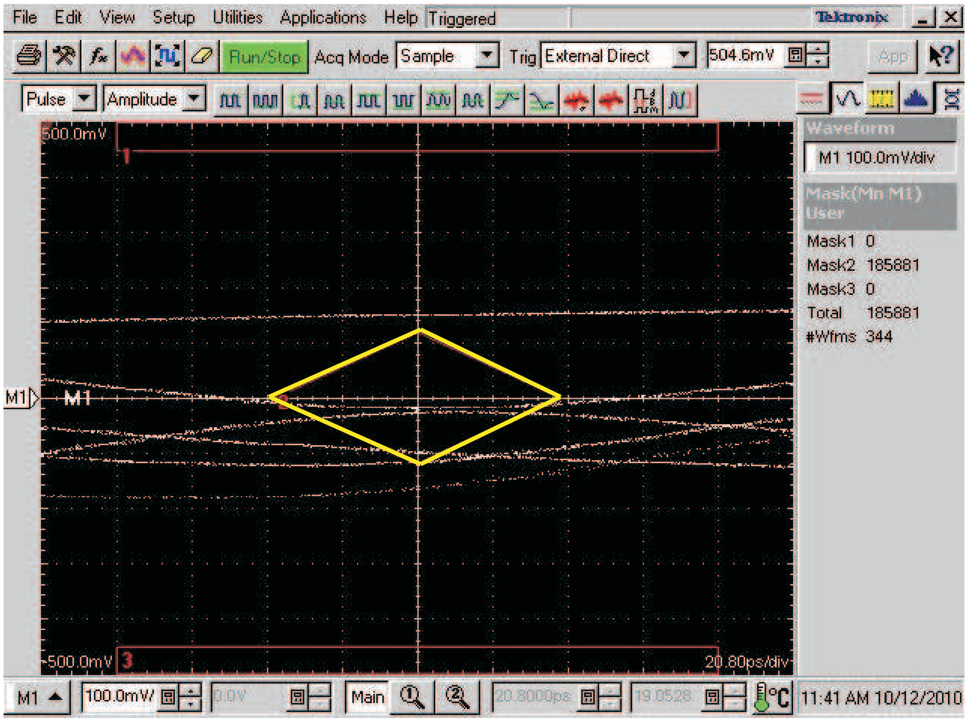
504.6mV

M1 100.0mV/div

Mask1 0
Mask2 0
Mask3 0
Total 0
#Wfms 210

M1 100.0mV 0.0V 20.8000ps 19.1110 11:33 AM 10/12/2010

Figure 17. Eye Pattern at B→ X= 24”; Y = 2” DE = 1 EQ = 0



Acq Mode Sample

Trig External Direct

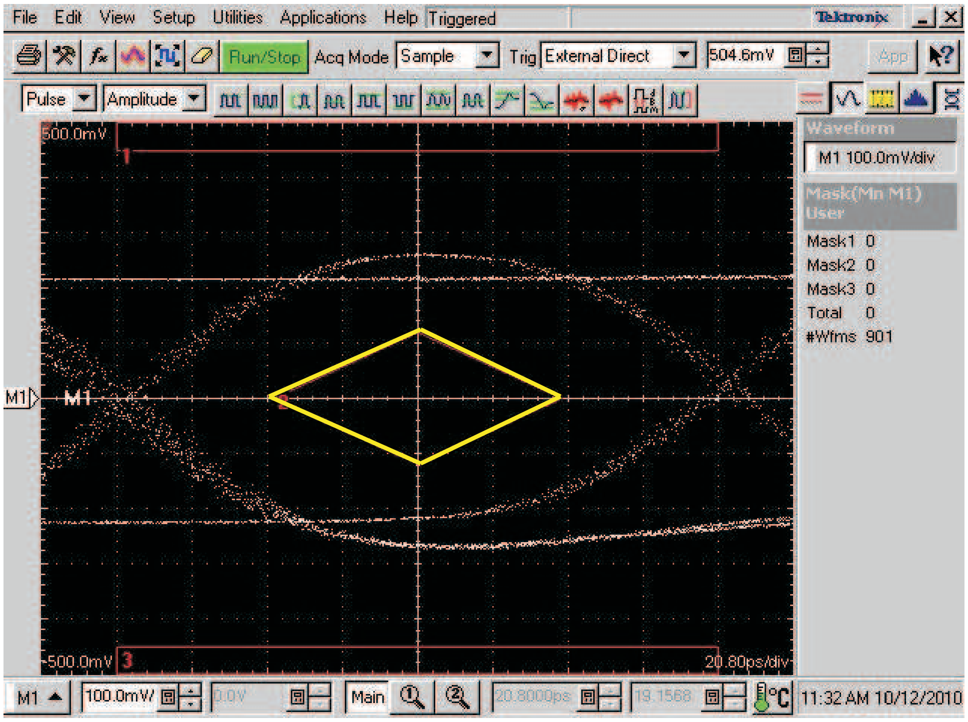
504.6mV

M1 100.0mV/div

Mask1 0
Mask2 185881
Mask3 0
Total 185881
#Wfms 344

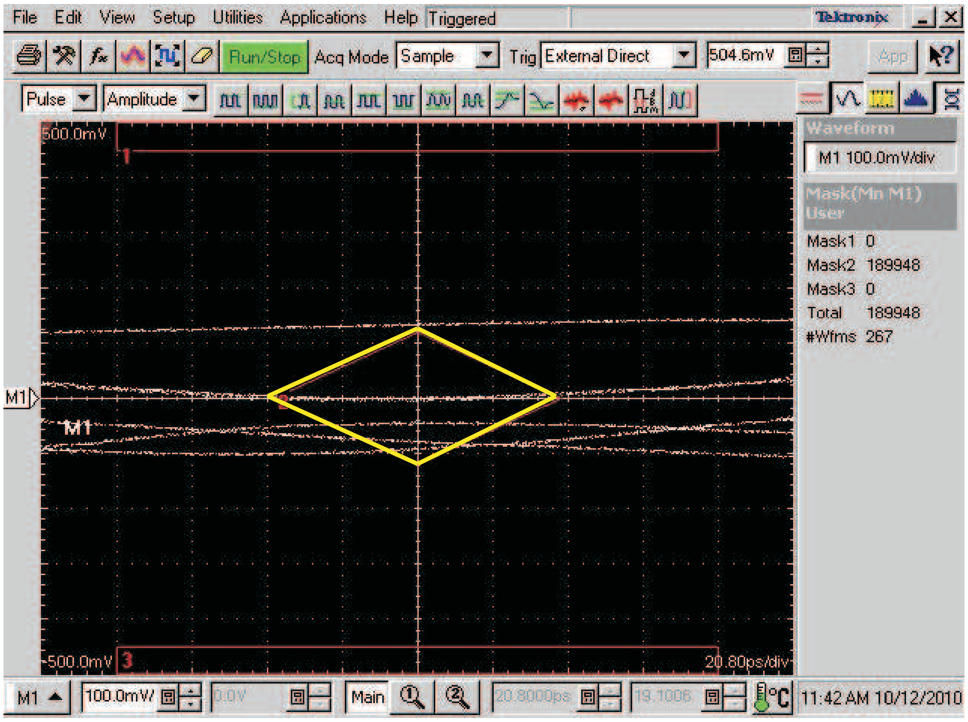
M1 100.0mV 0.0V 20.8000ps 19.0528 11:41 AM 10/12/2010

Figure 18. Eye Pattern at A → X= 32”; Y = 2” DE = 1 EQ = 1



Acq Mode Sample
Trig External Direct
504.6mV
M1 100.0mV/div
Mask1 0
Mask2 0
Mask3 0
Total 0
#Wfms 901
500.0mV
-500.0mV
20.80ps/div
M1 100.0mV/
0.0V
20.8000ps
19.1568
11:32 AM 10/12/2010

Figure 19. Eye Pattern at B → X= 32”; Y = 2” DE = 1 EQ = 1



Acq Mode Sample
Trig External Direct
504.6mV
M1 100.0mV/div
Mask1 0
Mask2 189948
Mask3 0
Total 189948
#Wfms 267
500.0mV
-500.0mV
20.80ps/div
M1 100.0mV/
0.0V
20.8000ps
19.1006
11:42 AM 10/12/2010

Figure 20. Eye Pattern at A → X= 40”; Y = 2” DE = 1 EQ = 1

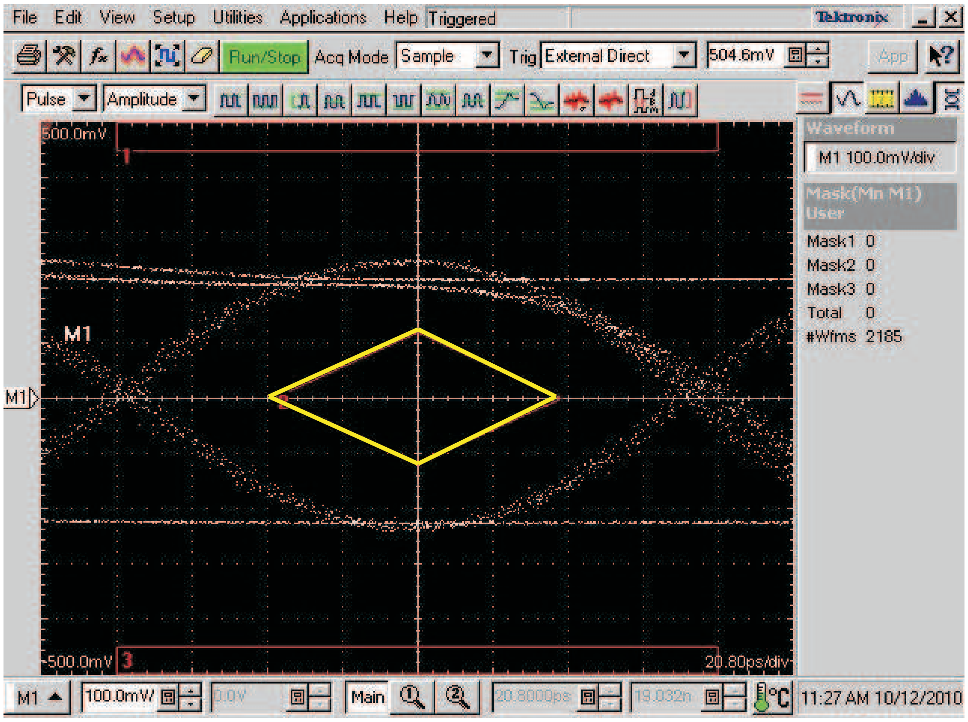


Figure 21. Eye Pattern at B → X= 40”; Y = 2” DE = 1 EQ = 1

DETERMINISTIC JITTER
vs
DATA RATE

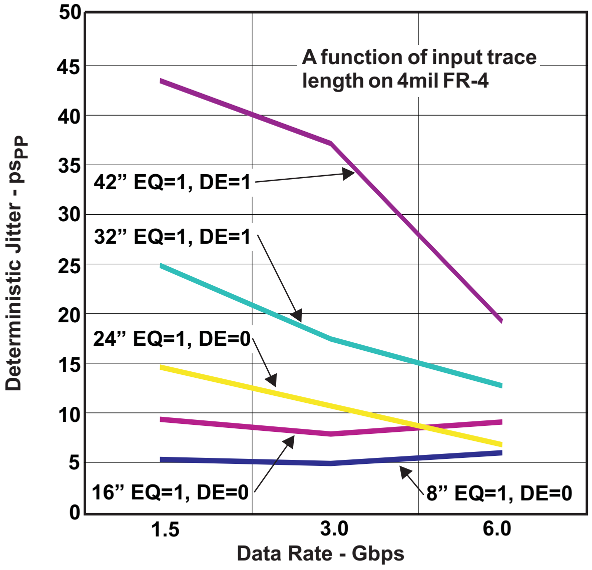


Figure 22.

DETERMINISTIC JITTER
vs
LAUNCH AMPLITUDE

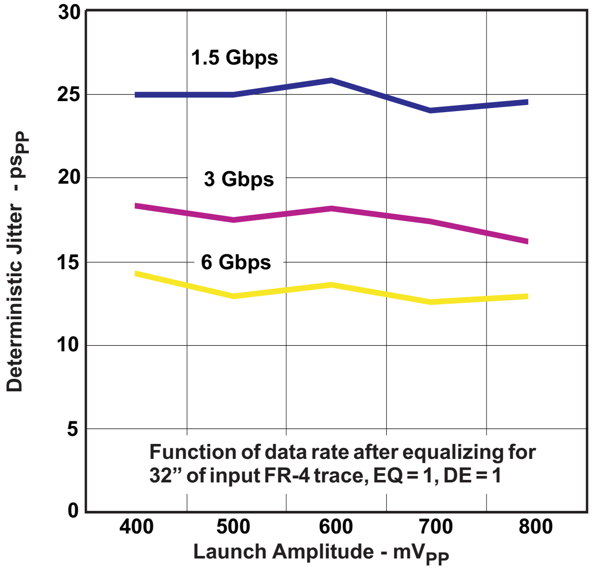


Figure 23.

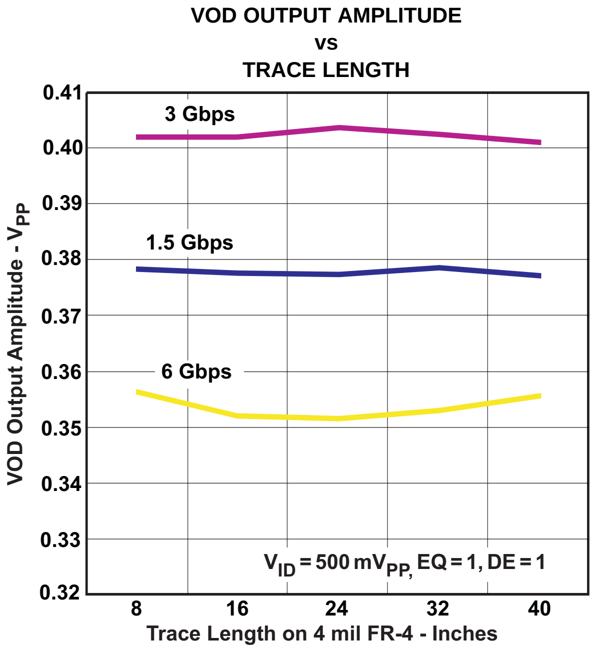

VOD OUTPUT AMPLITUDE
vs
TRACE LENGTH
VOD Output Amplitude - VPP
0.41
0.40
0.39
0.38
0.37
0.36
0.35
0.34
0.33
0.32
3 Gbps
1.5 Gbps
6 Gbps
VID = 500 mVPP, EQ = 1, DE = 1
8
16
24
32
40
Trace Length on 4 mil FR-4 - Inches

Figure 24.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75LVCP600DRFR	ACTIVE	WSON	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	600	Samples
SN75LVCP600DRFT	ACTIVE	WSON	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	600	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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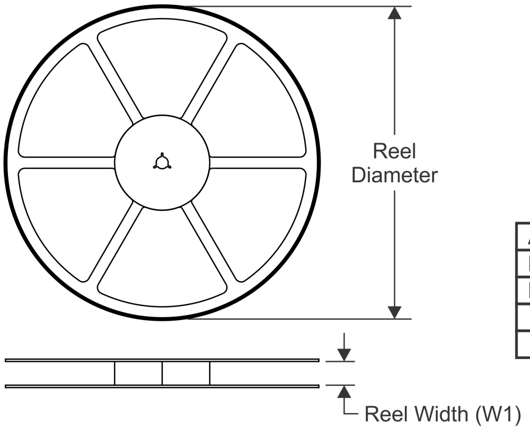
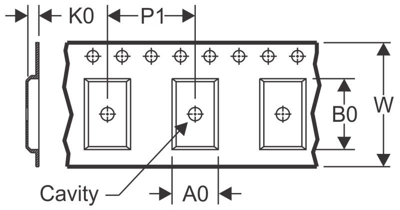
TAPE AND REEL INFORMATION

REEL DIMENSIONS

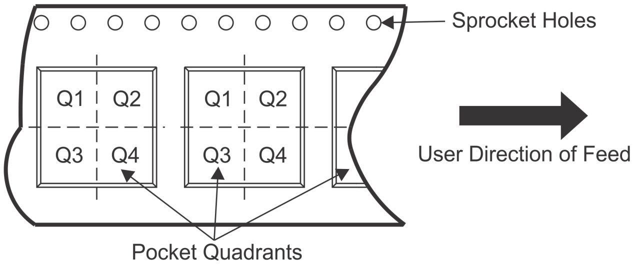


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

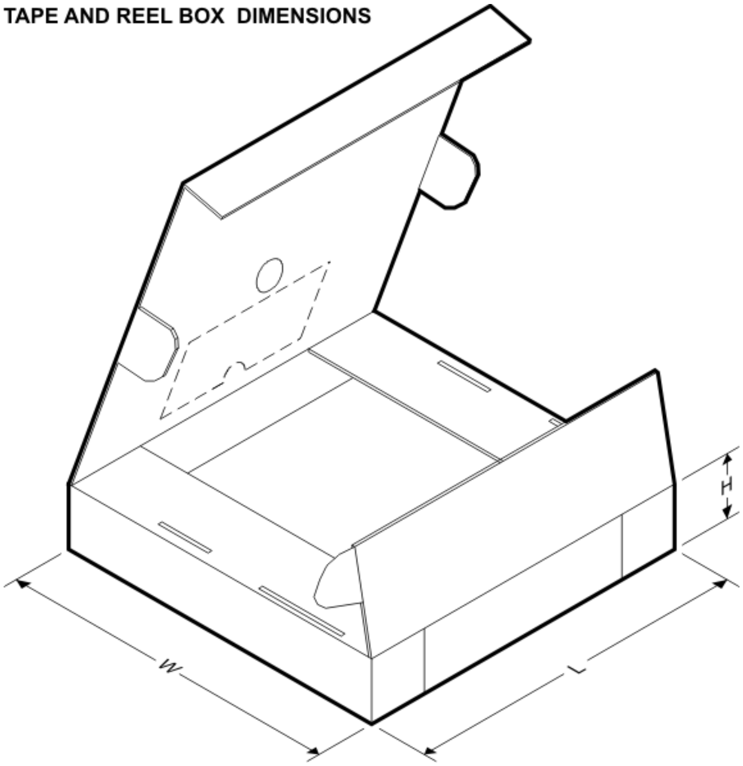
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP600DRFR	WSON	DRF	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
SN75LVCP600DRFT	WSON	DRF	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

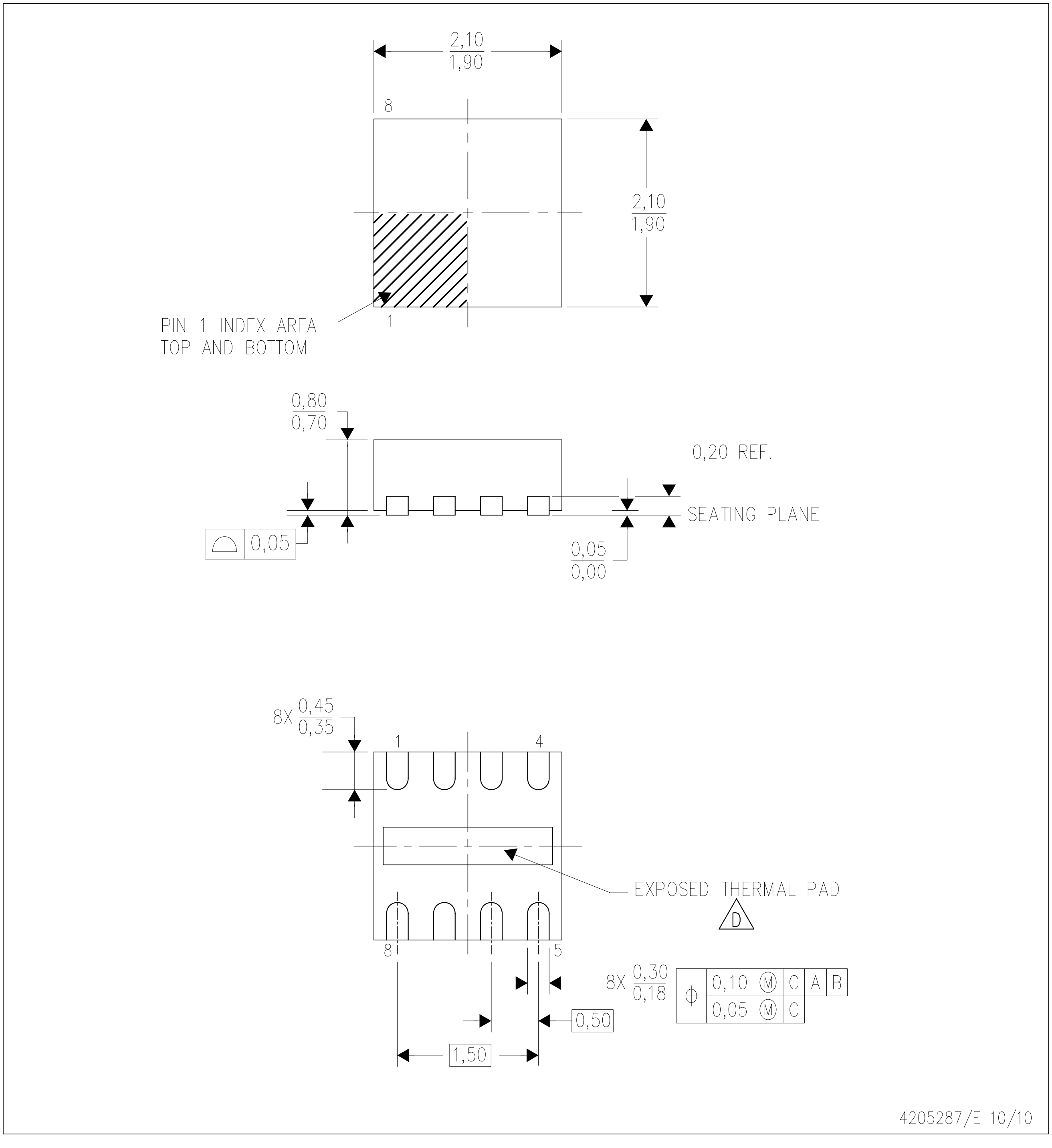
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP600DRFR	WSON	DRF	8	3000	210.0	185.0	35.0
SN75LVCP600DRFT	WSON	DRF	8	250	210.0	185.0	35.0

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–Leads (QFN) package configuration.
- D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–229.

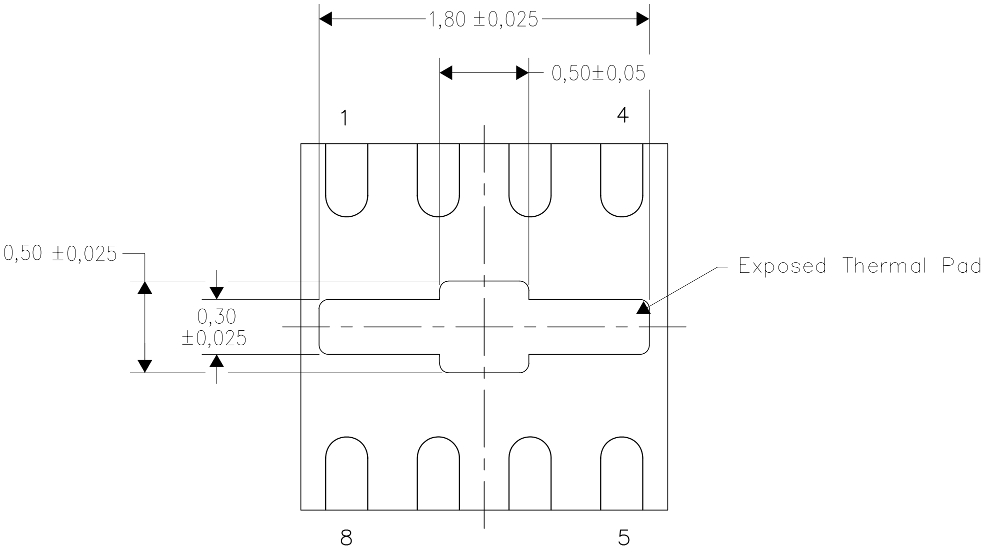
DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



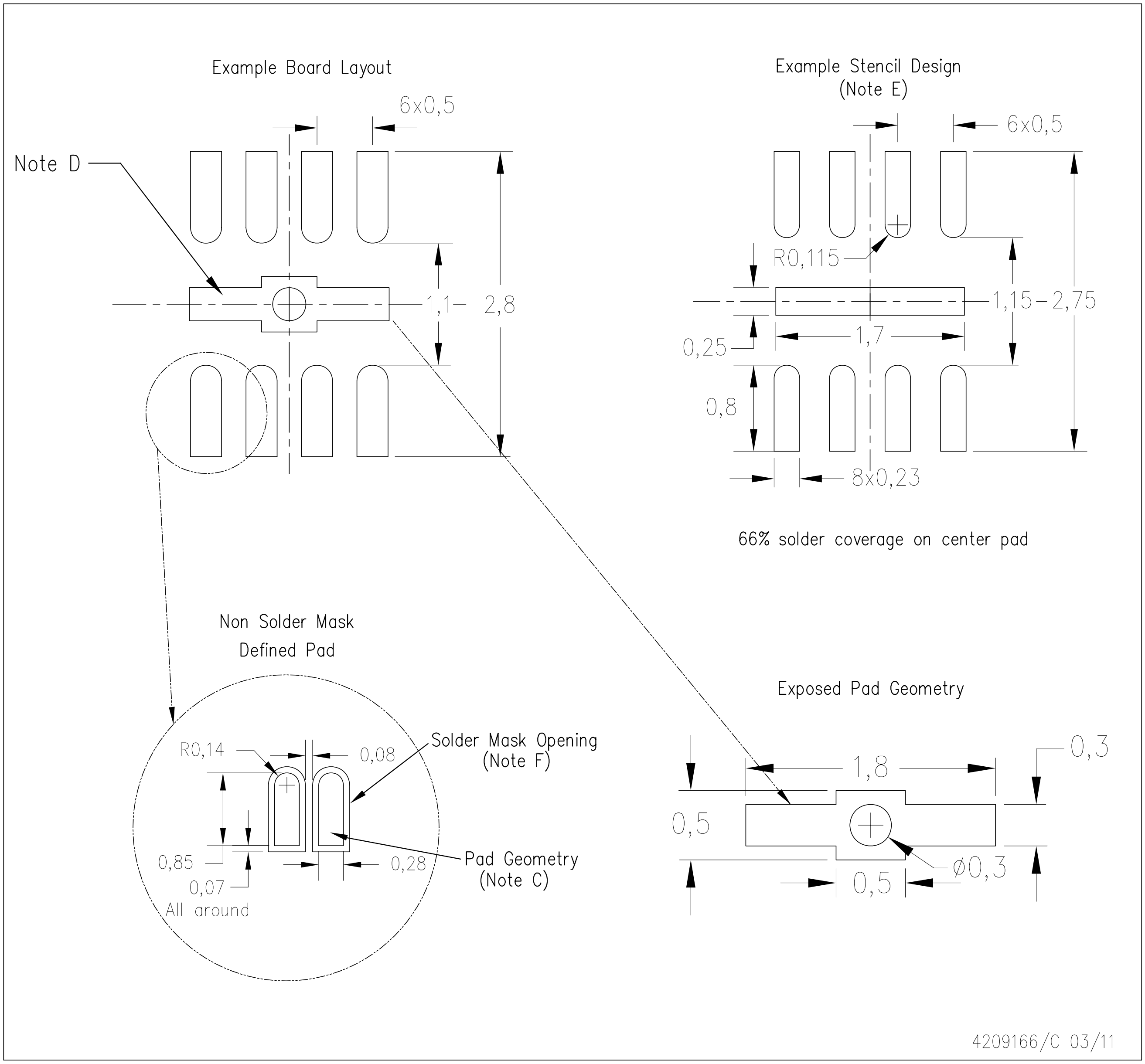
Bottom View

Exposed Thermal Pad Dimensions

4206840/G 04/11

NOTE: A. All linear dimensions are in millimeters

DRF (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



4209166/C 03/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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