PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1666B (HIGH Z)

SP1667B (LOW Z)

DUAL CLOCKED R-S FLIP-FLOP

Two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage.

The device is useful as a high-speed dual storage element.

TRUTH TABLE

S	R	C	Q_{n+1}
ø	ø	0	Q_n
0	0	1	Q_n
1	0	1	0
0	1	1	0
1	1	1	N.D.

ø = Don't care
N.D. = Not Defined

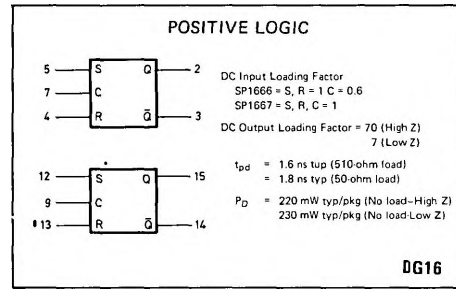


Fig. 1 Logic diagram of SP1666/1667

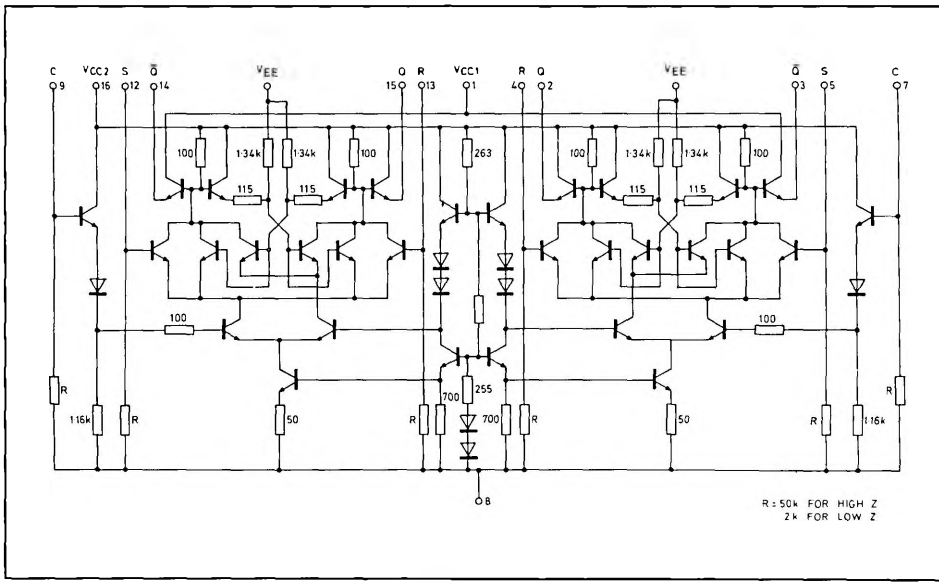


Fig. 2 Circuit diagram

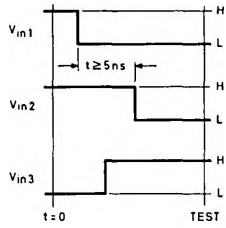
ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-14A2CB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is in either a test socket or is mounted on a printed circuit board.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1666/SP1667 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E(Hi-Z) ①	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
	I_E(Lo-Z) ①	8	–	–	–	60	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current (Hi-Z)	$I_{in\ H}$	12	–	–	–	0.370	–	–	mAdc	9,12	–	–	–	8	1,16
		13	–	–	–	0.370	–	–	mAdc	9,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	$I_{in\ L}$	12	–	–	0.500	–	–	–	μAdc	–	12	–	–	8	1,16
		9,13	–	–	0.500	–	–	–	μAdc	–	9,13	–	–	8	1,16
Input Current (Lo-Z)	$I_{in\ H}$	12	–	–	–	3.1	–	–	mAdc	9,12	–	–	–	8	1,16
		9,13	–	–	–	3.1	–	–	mAdc	9,13	–	–	–	8	1,16
	$I_{in\ L}$	12	–	–	1.300	–	–	–	mAdc	–	12	–	–	8	1,16
		9,13	–	–	1.300	–	–	–	mAdc	–	9,13	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ②	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	13	–	–	8	1,16
		15 ③	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	15 ④	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	–	12	–	–	8	1,16
		15 ⑤	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	14 ④	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	–	12	–	–	8	1,16
		14 ⑤	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	14 ②	−1.870	−1.635	−1.850	−1.920	−1.830	−1.595	Vdc	–	13	–	–	8	1,16
		14 ③	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15 ⑥	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	−1.020	–	−0.980	–	−0.920	–	Vdc	–	13	9	–	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15 ⑥	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	13	12	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OHA}	14 ⑥	−1.020	–	−0.980	–	−0.920	–	Vdc	–	–	13	12	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	14 ⑥	–	−1.615	–	−1.600	–	−1.575	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	−1.615	–	−1.600	–	−1.575	Vdc	–	13	9	–	8	1,16
Switching Times (50Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In	Pulse Out			−3.2V	+2.0V
Clock Input	t_{9+15+}	15	1.0	2.5	1.0	2.5	1.1	2.7	ns	9	15	–	–	8	1,16
	t_{9+15-}	15	↓	↓	↓	↓	↓	↓		↓	15	–	–	↓	↓
	t_{9+14-}	14									14	–	–		
	t_{9+14+}	14									14	–	–		
Set Input	t_{12+15+}	15	1.0	2.3	1.0	2.3	1.1	2.6	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	1.0	2.3	1.0	2.3	1.1	2.6	ns	12	14	–	–	8	1,16
Reset Input	t_{13+15-}	14	1.0	2.3	1.0	2.3	1.1	2.6	ns	13	14	–	–	8	1,16
	t_{13+14+}	15	1.0	2.3	1.0	2.3	1.1	2.6	ns	13	15	–	–	8	1,16
Rise Time	t_+	14,15	0.8	2.5	0.8	2.5	0.9	2.8	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.2	0.5	2.2	0.6	2.6	ns	9	14,15	–	–	8	1,16

(1) I_E is measured with no output pull-down resistors.



(2) Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} ro S (V_{IH} to V_{IL})

(3) Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to S (V_{IL} to V_{IL})

(4) Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

(5) Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

(6) Apply V_{in3} to C (V_{IH} to V_{IL})

(7) Apply V_{in3} to S (V_{IH} to V_{IL})

Fig. 3 Notes referred to in electrical characterstics

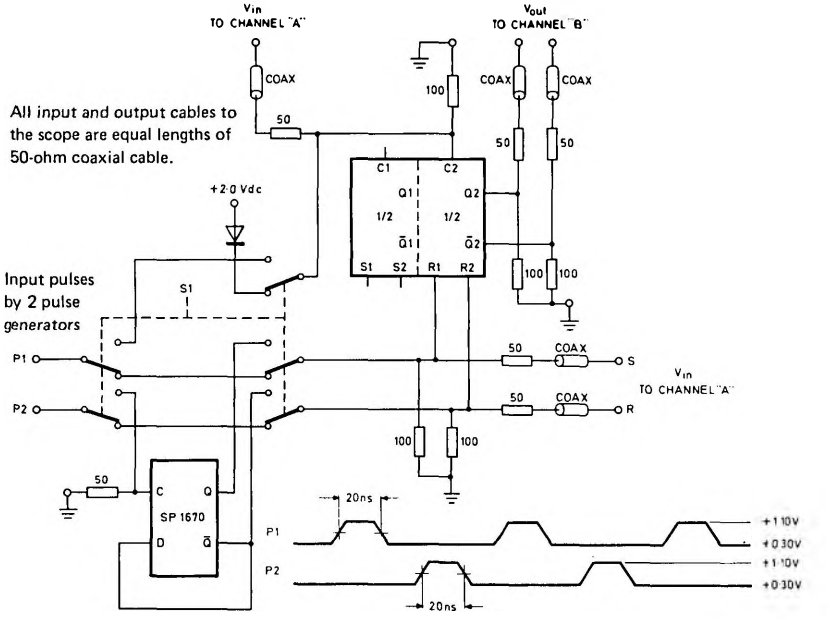


Fig. 4 Switching time test circuit

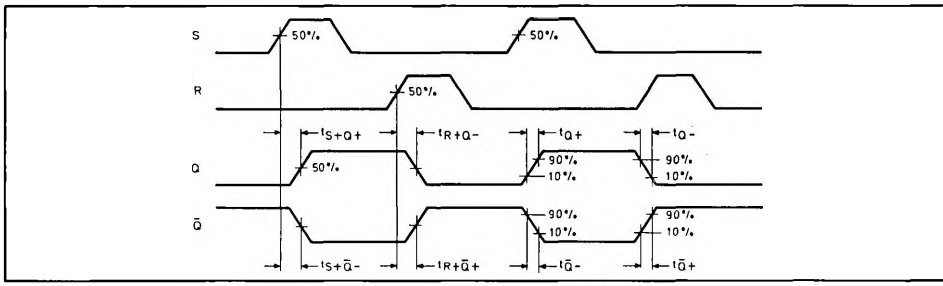


Fig. 5 Switching time waveforms (set/reset to Q/$\bar{Q}$, switch S1 in position shown in Fig. 4)

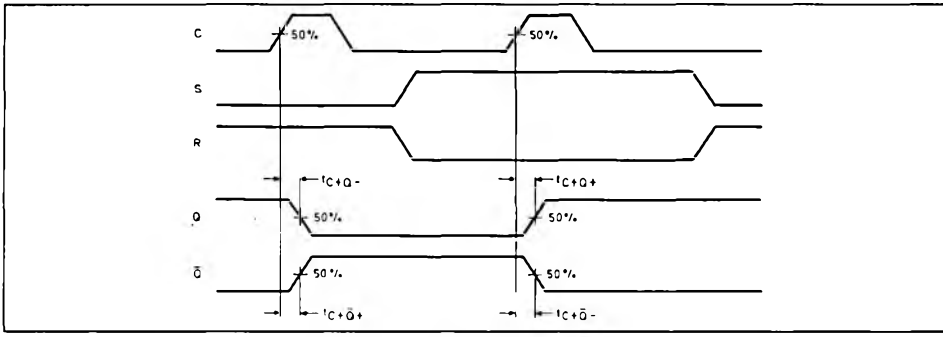


Fig. 6 Switching time waveforms (clock to Q/$\bar{Q}$, switch S1 in opposite position to that shown in Fig. 4)