SP5070

2.GHz Fixed Modulus Frequency Synthesiser

DS3966-2.2 May 996

The SP5070 is a single modulus frequency synthesiser for use in Satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only an external transistor is required for varicap line driving.

FEATURES

- Low Power Consumption (5V, 47mA typ.)
- Prescaler and Preamplifier Included
- Charge Pump Amplifier with Feedback Point
- Charge Pump Disable Facility
- Synthesises Frequencies up to 2.4GHz
- Pin and Function Compatible with SP5060 and SP5062
- Full ESD Protection*

  * Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems
- C-Band with Frequency Doubling Mixer

ORDERING INFORMATION

SP5070 DP - (14 Lead Plastic Package)
SP5070F MP - (14 Lead Miniature Plastic Package)

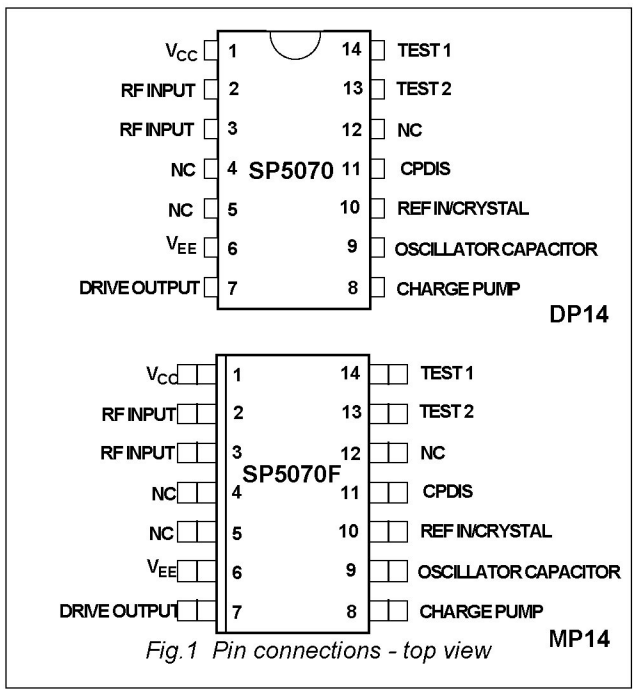


Fig.1 Pin connections - top view

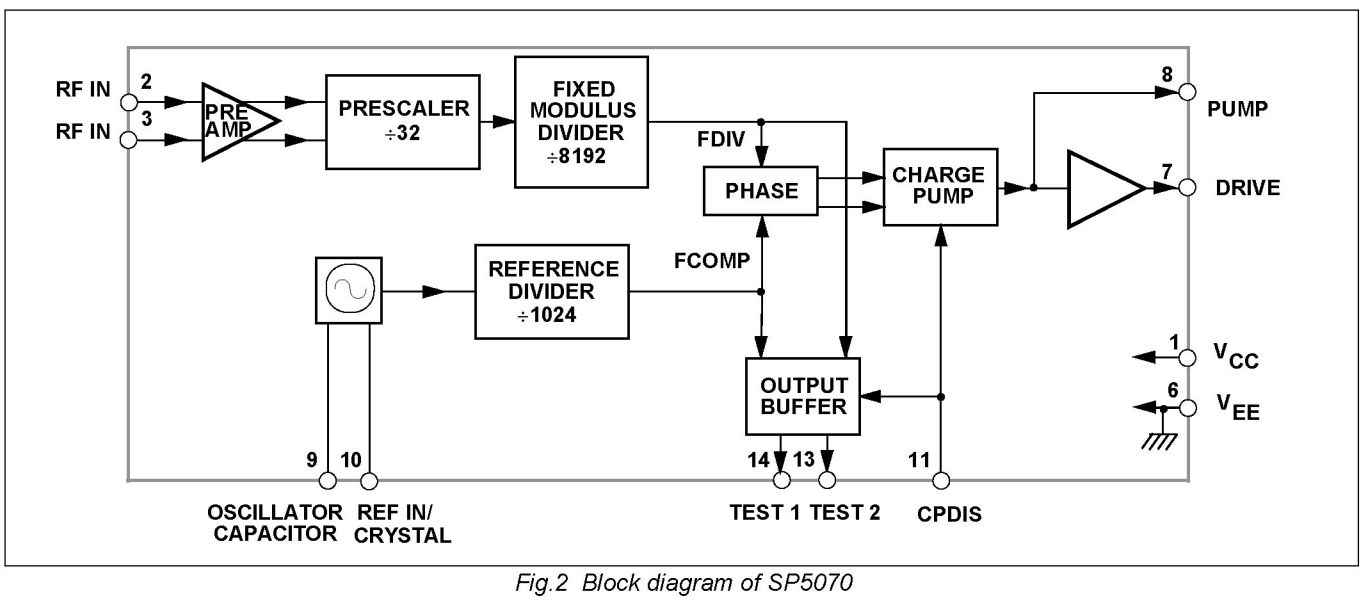


Fig.2 Block diagram of SP5070

ELECTRICAL CHARACTERISTICS

Tamb = -40°C to +85°C,VCC = +4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	1	-	47	55	mA	V_{CC} = 5V
Prescaler input voltage Prescaler input voltage		2,3 2,3	50 100	- -	300 300	mV_{RMS} mV_{RMS}	300MHz to 1.8GHz sinewave 2.4GHz, see Fig.5
Prescaler input impedance Input capacitance		2,3 2,3	- -	50 2	- -	Ω pF	
Charge pump output current Charge pump output leakage Drift due to leakage Charge pump drive output current Charge pump amplifier gain		8 8 - 7 -	- - - 1 -	±100 - - - 6400	- ±5 5 - -	µA nA mV/s mA -	V pin 8 = 2.0V V pin 8 = 2.0V At collector of External Varicap Drive transistor V pin 7 = 0.7V pin 7 current 100µa
Oscillator temperature stability Oscillator stability with supply voltage		9,10 9,10	- -	- -	2 2	ppm/°C ppm/V	
Reference clock frequency External reference amplitude		10 10	2 150	- -	10 500	MHz mV_{RMS}	
Charge pump disable/TEST 1 and TEST 2/enable Charge pump disable leakage		11 11	-250 -	- -	-500 10	µA µA	V_{IN}<0V V pin 11= V_{CC}
TEST 1/TEST 2 sink current		13,14	1	-	-	mA	VOUT = 0.7V
TEST 1/TEST 2 leakage current		13,14	-	-	10	µA	VOUT = V_{CC}+0.3V
TEST 1/TEST 2 voltage		13,14	-	-	V_{CC}+0.3	V	

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Characteristics	Pin	Value		Units
		Min	Max	
Supply voltage	1	-0.3	7	V
RF input voltage	2,3	-	2.5	Vp-p
RF input DC offset	2,3	-0.3	V_{CC}+0.3	V
Charge pump DC offset	8	-0.3	V_{CC}+0.3	V
Charge pump disable	11	-0.7	V_{CC}+0.3	V
Drive DC offset	7	-0.3	V_{CC}+0.3	V
Crystal oscillator DC offset	9,10	-0.3	V_{CC}+0.3	V
TEST outputs	13,14	-0.3	V_{CC}+0.3	V
Storage temperature	-	-55	150	°C
Junction temperature	-	-	+150	°C
DP14 thermal resistance, chip-to-ambient	-	-	78	°C/W
DP14 thermal resistance, chip-to-case	-	-	30	°C/W
MP14 thermal resistance, chip-to-ambient	-	-	123	°C/W
MP14 thermal resistance, chip-to-case	-	-	45	°C/W
Power consumption at 5.5V	-	-	275	mW

FUNCTIONAL DESCRIPTION

The SP5070, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator comparison frequency is obtained by dividing the reference frequency. This may be generated on-chip by means of an external crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phased locked to the comparison frequency.

The divider stages are arranged to give a fixed ratio between the synthesised frequency and the reference of 256:1. Any frequency within the range of 300MHz to 2.4GHz may be achieved by using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output drive necessary for the oscillator varicap line.

A test facility which disables the charge pump is also provided. This is activated when a negative voltage is applied to pin 11, see electrical characteristics above. When the device is in this mode, F_{COMP} and F_{DIV} are also available at outputs TEST1 and TEST2 respectively. These are open collector outputs and are each capable of sinking a minimum of 1mA. In normal mode of operation these outputs are high impedance.

For compatibility with SP5060/SP5062, pin 11 may be connected toV_{CC}

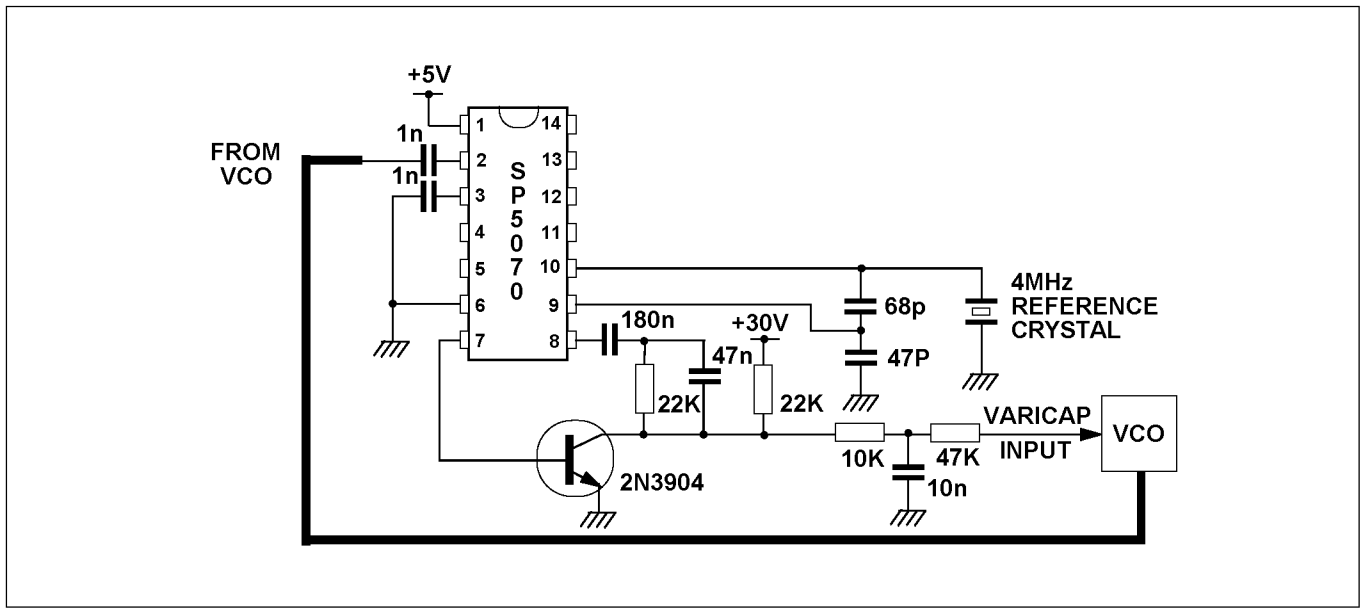


Fig.3 Typical application and test circuit (1024MHz with 4MHz reference crystal)

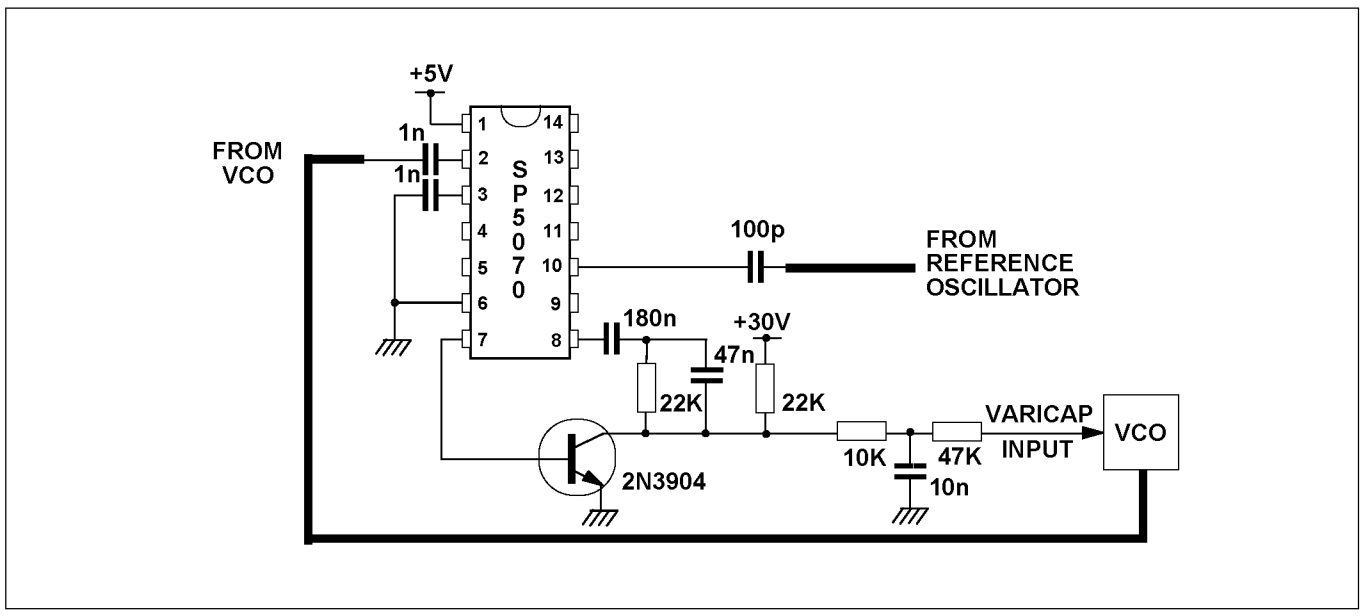


Fig.4 Application using external reference oscillator

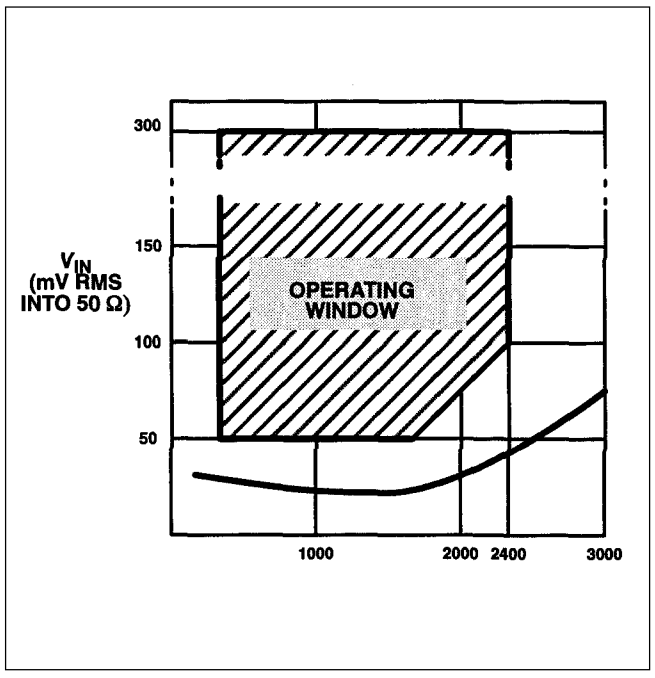


Fig.5 Typical input sensitivity

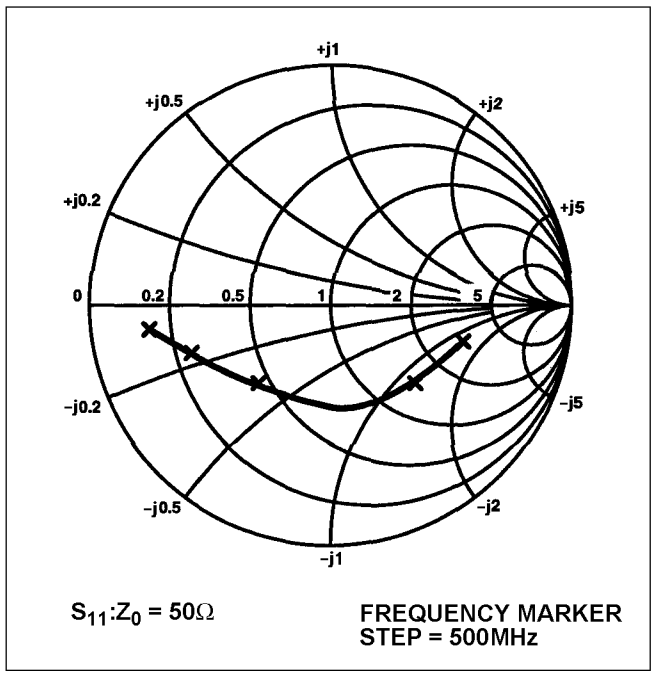


Fig.6 Typical input impedance

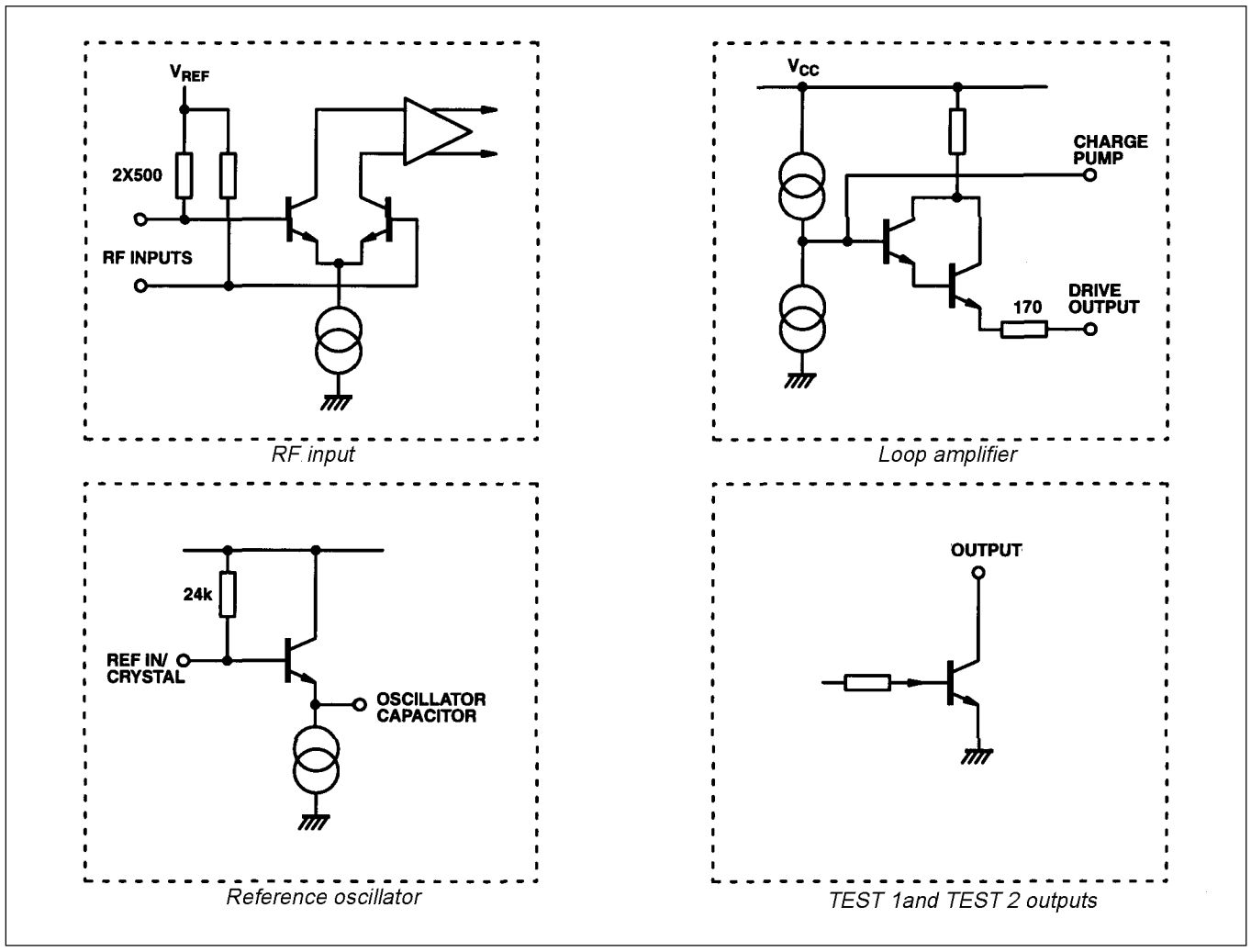
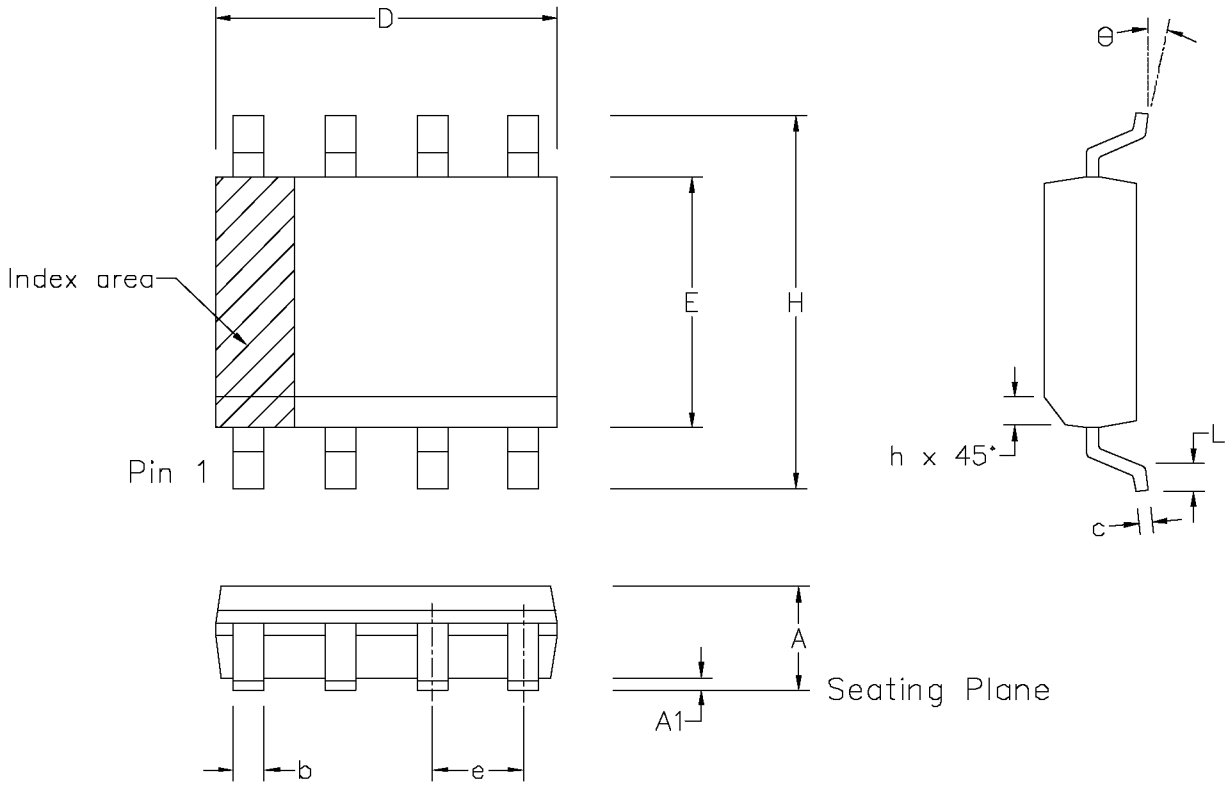


Fig.7 SP5070 input/output interface circuits



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
Θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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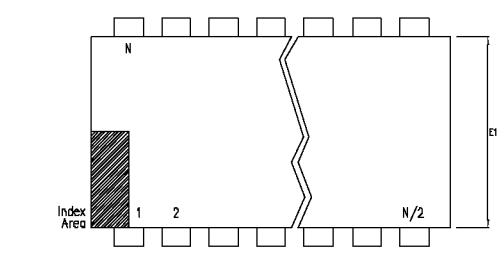
ORIGINATING SITE: SWINDON

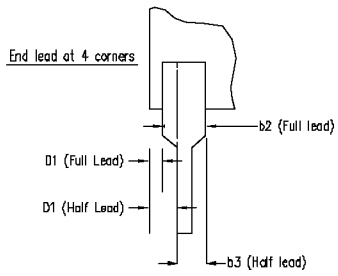
ISSUE	1	2	3	4	
ACN	006745	201937	202596	203707	
DATE	7APR95	27FEB97	12JUN97	9DEC97	
APPROVED					

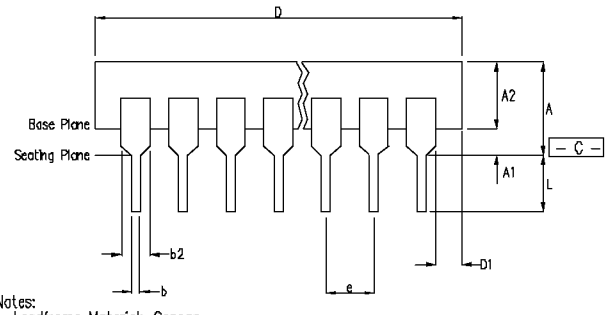
MITEL SEMICONDUCTOR

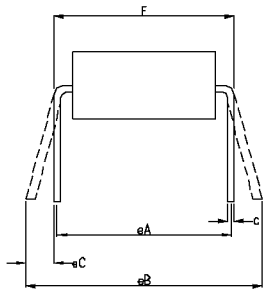
Title: Package Outline Drawing for 14 lds SOIC(N)-0.150" Body Width (MP)

Drawing Number
GPD00011









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	18.67	19.69	0.735	0.775
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	14		14	
Conforms to Jedec MS-001AA Issue D				

Notes:
1. Leadframe Material: Copper
2. Leadframe finish: Solder Plate
3. Dimensions D, D1 & E1 do not include mould flash or protrusions.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
5 Dimensions eB & eC are measured with the leads unconstrained
6 Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
7. N is the maximum of terminal positions.

This drawing supersedes:–
Lincoln drawing # XG4B9
Oldham drawing # TD/D 609
Roborough/Swindon drawing # 41B/ED/39502/002

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ORIGINATING SITE: Swindon

ISSUE	1					MITEL SEMICONDUCTOR
ACN	202539					
DATE	23MAY97					
APPROVED						

Title:
14 Lead Plastic DIP Outline Drawing

Drawing Number
GPD00344

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