PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH-SPEED DIVIDERS

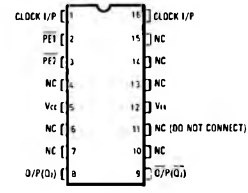
SP 8725 A, B & M
UHF PROGRAMMABLE DIVIDER 300MHz ÷ 3/4

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8725 series are UHF integrated circuits that can be logically programmed to divide by either 3 or 4 with input frequencies up to 300MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

All inputs and outputs are ECL-compatible throughout the temperature range: the clock inputs and programming inputs are ECL10K-compatible while the two complementary outputs are ECLII-compatible to reduce power consumption in the output stage. ECL 10K output compatibility can be achieved very simply, however (see Operating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 3 when either $\overline{PE}$ input is in the high state and by 4 when both inputs are in the low state. Both the PE inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).



DC16 DG16

NOTE: UNUSED PINS (EXCEPT 8 AND 9) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. PINS 8 AND 9 SHOULD BE LEFT OPEN-CIRCUIT WHEN NOT IN USE. PIN 11 IS INTERNALLY CONNECTED AND MUST ALWAYS BE LEFT OPEN-CIRCUIT.

Fig. 1 Pin connections (top)

FEATURES

- Military and Industrial Variants
- 300 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps and O/Ps
- Low Propagation Delay
- True and Inverse Outputs

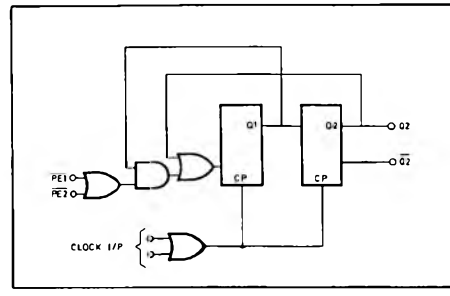


Fig. 2 Logic diagram (positive logic)

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to +70°C
  'M' Grade −40°C to +85°C
- Supply Voltage | Vcc - V_{EE} | 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

ABSOLUTE MAXIMUM RATINGS

Supply voltage |Vcc − V_{EE}|	8V
Input voltage V_{in} (d.c.)	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: 'A' Grade −55°C to +125°C
'B' Grade 0°C to +70°C
'M' Grade −40°C to 85°C
Supply coltage (see note 1): V_{CC} = 0V
V_{EE} = −5.2V

Static Characteristics

Charactistic	Value Min	Typ.	Max.	Units	Conditions
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see note
Input pulldown resistance, between pins 1, 2, 3 and 16 and V_{EE} (pin 12)		4.3		k Ω	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2k Ω pulldown resistor on each output)
Power supply drain current		45	60	mA	

NOTES
1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

Dynamic Characteristics

Characteristic	Value Min.	Typ.	Max.	Units	Conditions
Clock input voltage levels					
V_{INH}	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	−1.70		−1.50	V	see note 4
Max. toggle frequency	300			MHz	
Min. frequency with sinewave clock input			10	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz			20	V/μs	
Propagation delay (clock input to device output)		3		ns	
Set-up time		1.5		ns	See note 5
Release time		1.5		ns	See note 6

NOTES
4. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L → H transition of a control input and the next L → H clock pulse transition to ensure that the ÷3 mode is forced by that clock pulse (see Fig.3).
6. Release time is defined as the minimum time that can elapse between a H → L transition of a control input and the next L → H clock pulse transition to ensure that the ÷4 mode is forced by that clock pulse (see Fig. 4.)

OPERATING NOTES

The SP8725 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

The ÷3/4 requires ECL control logic at the maximum input frequency, but can be controlled by a TTL fully programmable counter at a reduced input clock frequency. When used the outputs and inputs must be interfaced to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7, gives the true output; the inverse can be obtained by interchanging the Q_2 and $\overline{Q_2}$ outputs. The output interface will operate satisfactorily over the full military temperature range (−55°C to +125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 200MHz this would only leave about 5ns for the fully programmable counter to control the ÷3/4. The loop delay can be increased by extending the ÷3/4 function to, say, ÷12/13 or ÷24/25.

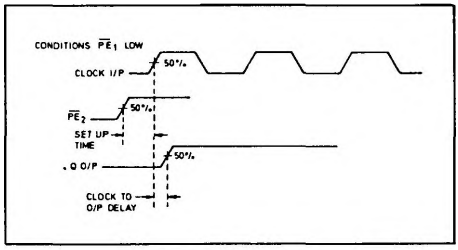


Fig. 3 Set-up timing diagram

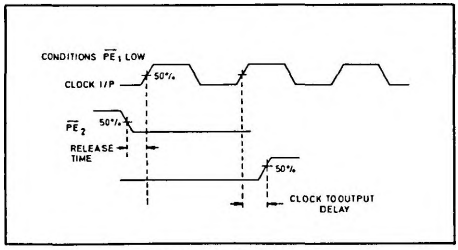


Fig. 4 Release timing diagram

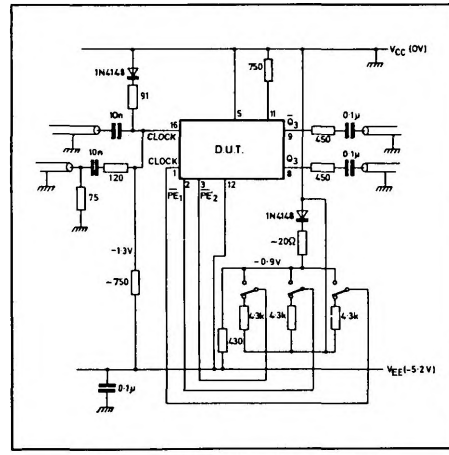


Fig. 5 Test circuit for dynamic measurements

Clock Pulse	Q_1	Q_2	
1	L	H	
2	L	L	
3	H	L	
4	H	H	←Extra State

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio.
L	L	4
H	L	3
L	H	3
H	H	3

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L→H transition from Q_2 or the H→L transition from $\overline{Q_2}$ is used to clock the stage controlling the ÷3/4 circuit. The loop delay is 3 clock periods minus the internal delays of the ÷3/4 circuit.

The SP8725 device O/Ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can also be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

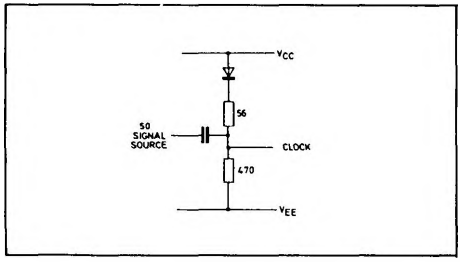


Fig 6. Recommended input bias configuration for capacitive coupling to a continuous 50 Ω signal source

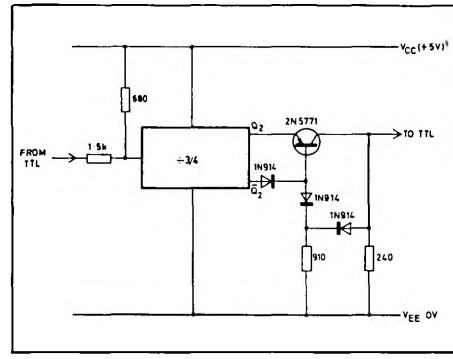


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8725 device and TTL operating from the same supply rails)

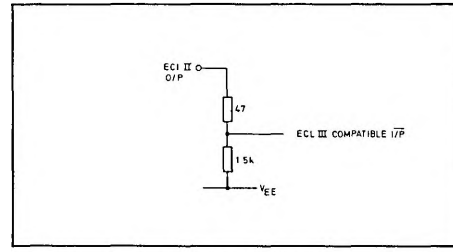


Fig. 8 ECL II to ECL III interface.

PACKAGE DETAILS

Dimensions are shown thus: mm(in)