

# SP 8741A, B & M

## AC COUPLED UHF PROGRAMMABLE DIVIDERS 300 MHz $\div$ 6/7

The SP8741 A, B & M are high speed  $\mu$ programmable  $\div$ 6/7 counters operating at an input frequency of up to 300 MHz over the temperature ranges  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  and  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two  $\overline{\text{PE}}$  inputs. The counter will divide by 6 when either input is in the high state, and by 7 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal  $4.3\text{k}\Omega$  internal pull-down resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-six prescaler the inverse output (o/p) should be connected to a PE input.

Clock Pulse	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
1	L	H	H
2	L	L	H
3	H	L	H
4	L	H	L
5	L	L	L
6	H	L	L
7	H	H	H

← Extra state

Table 1 Count sequence

$\overline{\text{PE}}_1$	$\overline{\text{PE}}_2$	Div Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Table 2 Truth table for control inputs

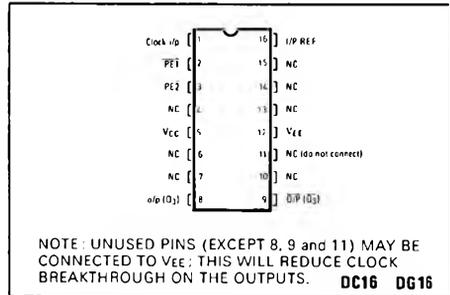


Fig. 1 Pin connections

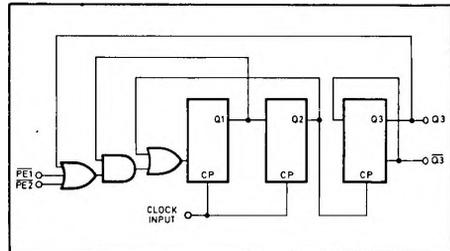


Fig. 2 Logic diagram

### FEATURES

- Full Temperature Range Operation
  - 'A' Grade  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
  - 'B' Grade  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$
  - 'M' Grade  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

### ABSOLUTE MAXIMUM RATINGS

Power supply voltage $ V_{CC} - V_{EE} $	0V to +8V
Input voltage, PE inputs	0V to $V_{CC}$
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	$+150^{\circ}\text{C}$
Storage temperature	$-55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$

# SP8741

## ELECTRICAL CHARACTERISTICS

$\overline{PE}$  inputs – ECL 10K compatible

Outputs – ECL II compatible

Test conditions (unless otherwise stated)

$T_{amb}$ : 'A' grade  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 'B' grade  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$   
 'M' grade  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

Supply voltages:  $V_{CC} = +5.2\text{V} \pm 0.25\text{V}$   
 $V_{EE} = 0\text{V}$

Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	300			MHz	$V_{CC} = +5.2\text{V}$ Sinewave Input
Min i/p frequency			40		
Min. slew rate for square wave input			100	V/ $\mu\text{s}$	
Propagation delay (clock i/p to device o/p)		4		ns	$V_{CC} = +5.2\text{V}, 25^{\circ}\text{C}$ $V_{CC} = +5.2\text{V}, 25^{\circ}\text{C}$
$\overline{PE}$ input reference level		+3.9		V	
Power supply drain current		45	60	mA	
$\overline{PE}$ input pulldown					
Resistors		4.3		$\text{K}\Omega$	
Clock i/p impedance (i/p to i/p ref low frequency)		400		$\Omega$	

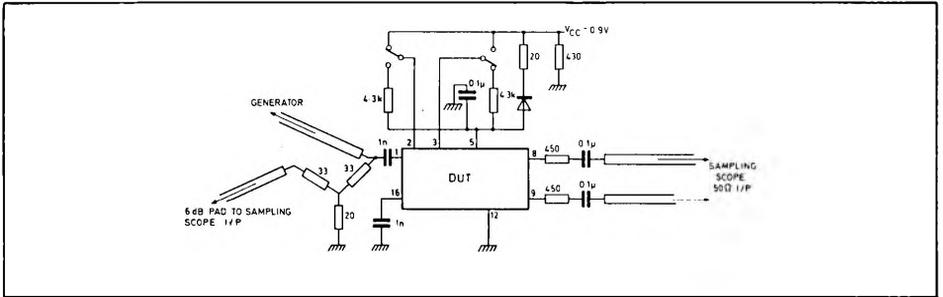


Fig. 3 Test circuit

## APPLICATION NOTES

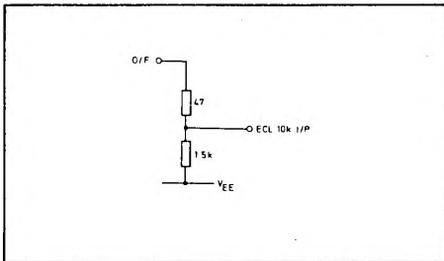


Fig. 4

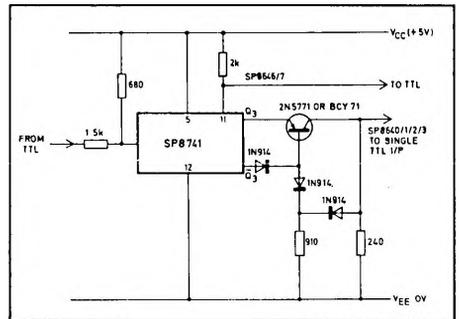


Fig. 5

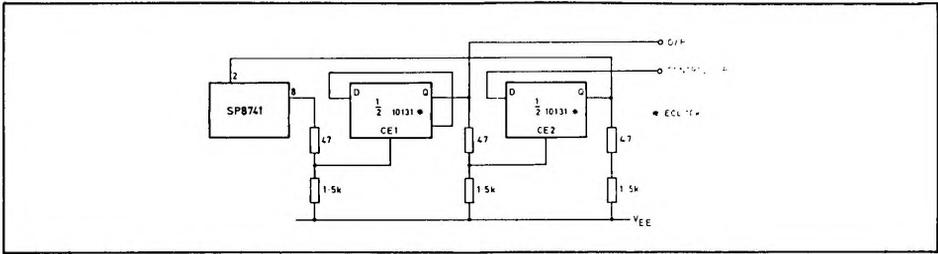


Fig. 6 Divide-by-12/14. Control loop delay time approximately 40ns.

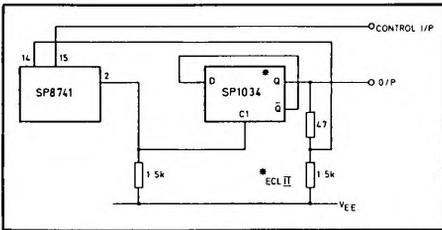


Fig. 7 Divide-by-12/13. Control loop delay time approximately 30ns using SP1034.

When operating the SP8741 in a synthesiser loop at 300MHz the delay time through the programmable divider controlling the SP8741 is approximately 16ns. As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8741 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the  $\overline{PE}$  pins, and the output of the SP8741 into TTL, is shown in Fig. 5.