PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8790 A, B & M

÷ EXTENDER FOR 2-MODULUS COUNTERS

The SP8790 is a divide-by-four counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide-by-10 or 11 with the SP8790 becomes a divide-by-40 or 41, a divide by 5 or 6 becomes a divide by 20 or 21.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8790 into the region where CMOS or low power TTL can control the divider. The power-saving advantages are obvious.

The device interfaces easily to the SP8690 range of divide by 10 or 11s. The control inputs are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8790 is available in three temperature grades: 0°C to +70°C (SP8790B), −40°C to +85°C (SP8790-M) and −55°C to +125°C (SP8790A).

The SP8790 requires supplies of 0V and +5V ±0.25V.

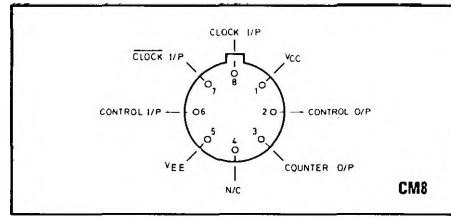

Fig. 1 Pin connections

FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- I/P and O/P Interface Direct to CMOS/TTL

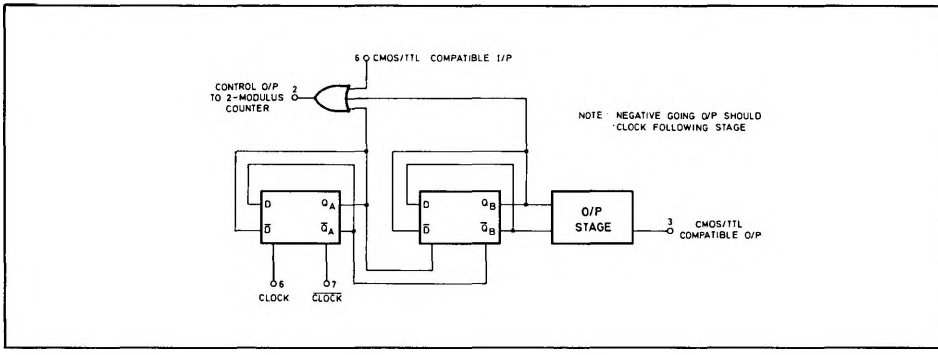

Fig. 2 Logic diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | VCC—VEE|	8V
DC input voltage	Not greater than supply
AC input voltage	2.5Vp-p
Output bias voltage	12V
Control input bias voltage	12V
Operating junction temperature	+150°C
Storage temp. range	−55°C to 150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: −55 C to −125 C (A grade)
−40 C to −85 C (M grade)
0 C to −70 C (B grade)
V_{CC} = −5V ± 5%
V_{EE} = 0V
Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Dynamic					
Toggle frequency	See note 1			MHz	
Min toggle frequency with sine-wave input			20	MHz	See note 2
Min toggle frequency with square wave input	0			Hz	Slew rate 50V/µs
Clock to O/P delay (O/P − ve going)		14		ns	
Clock to O/P delay (O/P + ve going)		28		ns	
Control I/P to control O/P delay (O/P−ve going)		20		ns	10kΩ pulldown on control O/P (See note 5)
Clock I/P to control O/P delay (O/P+ve going)		10		ns	10kΩ pulldown on control O/P (See note 5)
Control I/P to control O/P delay (O/P−ve going)		12		ns	4.3kΩ pulldown on control O/P (See note 6)
Control I/P to control O/P delay (O/P+ve going)		9		ns	4.3kΩ pulldown on control O/P (See note 6)
Clock to control O/P delay (O/P −ve going)		26		ns	10kΩ pulldown on control O/P (See note 5)
Clock to control O/P delay (O/P −ve going)		12		ns	10kΩ pulldown on control O/P (See note 5)
Clock to control O/P delay (O/P−ve going)		17		ns	4.3kΩ pulldown on control O/P (See note 6)
Clock to control O/P delay (O/P−ve going)		12		ns	4.3kΩ pulldown on control O/P (See note 6)
Static					
Control I/P voltage level					
High state	3.5		10	V	See note 3
Low state	0		1.5	V	
Output voltage level					
V_{OL}			0.4	V	Sink current = 6.0mA
V_{OH} (See note 4)					
Input impedance		1.6		kΩ	f_{in} = 0Hz
Input vias voltage ($\overline{CLOCK}$ and CLOCK)		2.4		V	Inputs open circuit
Power supply drain current		8.0	11	mA	

NOTES

1. The maximum frequency of operation is in excess of 60MHz when the SP8790 is used as a prescaler. The limitation on this maximum frequency is the saturating O/P stage. When the SP8790 is used as a controller its internal delays do not permit operation at frequencies in excess of 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. V_{OH} will be the supply voltage that the output pull-up resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695 with which the SP8790 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of the SP8640 series SP8745 and SP8746 with which the SP8790 can be used.

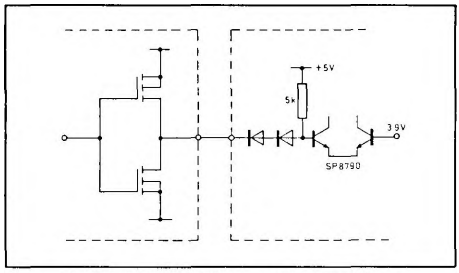

Fig. 3 CMOS and TTL compatible control input

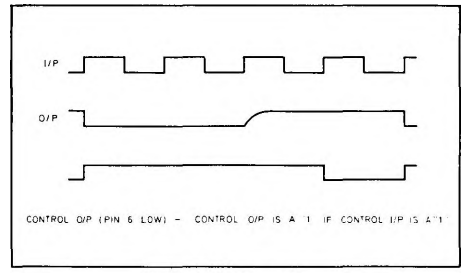

Fig. 4 SP8790 waveforms

OPERATING NOTES

The SP8790 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷40/41 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present. This may be prevented by using one of the arrangements shown in Fig. 6.

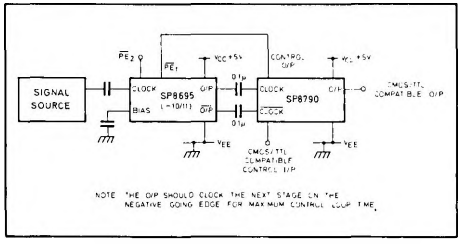

Fig. 5 SP8790 with SP8695 connected to give a ÷40/41

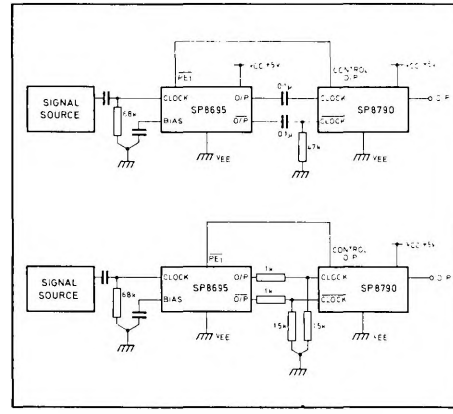

Fig. 6 Methods of preventing self-oscillation

TRUTH TABLE	
Control Input	**Div. Ratio With ÷10/11**
0	41
1	40

Max input frequency to combination=200MHz (min.).
Power consumption of combination=120mWtyp.
Time available to control the ÷40/41=(40 clock periods minus delays through the dividers) — 340ns (f_{in}=100MHz).