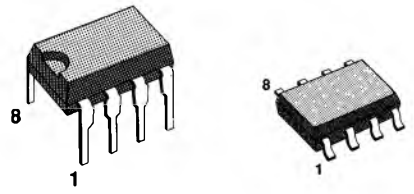
SGS-THOMSON MICROELECTRONICS

ST24C02A

2K BIT (256 X 8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

- 256 X 8 BIT ORGANIZATION.
- 2 WIRE SERIAL INTERFACE, COMPATIBLE WITH THE INTER-INTEGRATED CIRCUIT (I^2C) BUS.
- SINGLE POWER SUPPLY (READ AND WRITE)
- WORD AND MULTIBYTE WRITE CAPABILITY (UP TO 4 BYTES)
- PAGE WRITE CAPABILITY
- SELF-TIMED PROGRAMMING CYCLE
- AUTOMATIC WORD ADDRESS INCREMENTING.
- SEQUENTIAL REGISTER READ
- LOW POWER CMOS
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY
- OVER 1 MILLION ERASE/WRITE CYCLES
- OVER 10 YEARS DATA RETENTION



PDIP8 PSO8

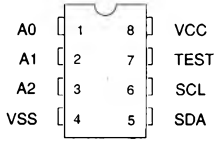
(Ordering information at the end of the datasheet)

PIN NAMES

A0-A1-A2	Address Inputs
VSS	Ground
SDA	Serial Data
SCL	Serial Clock
TEST	Test Input
V_{CC}	Power Supply

PIN CONNECTION

Dual-in-line Package - top view



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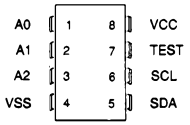
SO Package - top view



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DESCRIPTION

The ST24C02A is a 2048 read/write non volatile memory organized in 256 words of 8 bits and is manufactured in SGS-THOMSON highly reliable CMOS EEPROM technology.

It is an external memory accessed via a simple serial interface. This serial interface based on a two wire bus, allows bi-directional communication between devices.

The 2K bits memory capacity is divided in 256 registers of 8 bits. All memory operations are synchronized on an external strobe: SCL bus. The Read and Write operations are initiated by a Start instruction sent on the SDA bus by the master device.

The Start instruction includes a Start condition followed by an 8 bit word : the seven first bits address the right EEPROM slave device and the last bit defines the kind of operation to follow - Read or Write. A Start instruction is ended by an acknowledge of the slave device.
The specific address of a given ST24C02A is hardwired through the 3 address pins A0,A1 and A2.
The ST24C02A features 3 kind of operations:

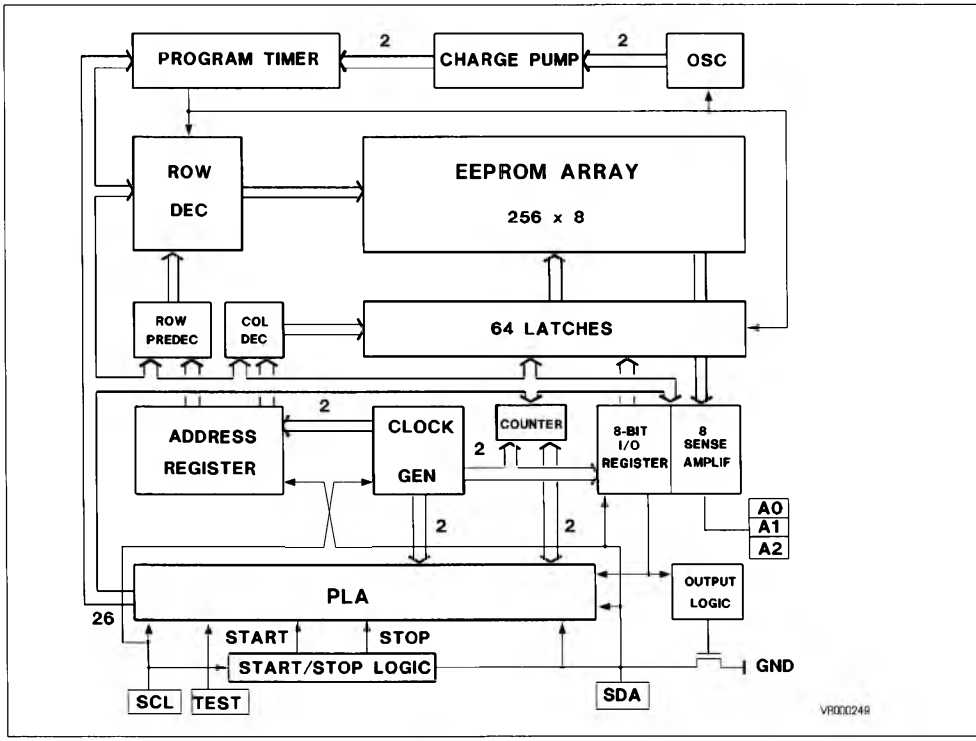
- Byte Write: 8 bits are written at the address previously defined in the byte write operation mode.
- Multibyte programming which allows to write consecutively up to 4 words in any location of the memory array in a single programming cycle.
- Page Write mode which allows to write from 2 to 8 bytes in a single programming cycle.

In Read Mode 3 read operations are available for the user:

- The Current Address read performs a read operation at the previously pointed address incremented by one.
- The Random Read realizes a read at the address defined in the random read instruction.
- The Sequential Read performs either a Current Address read or a Random Read, but reads consecutive words provided the master device acknowledges each string of 8 bits read from the memory without generating a STOP condition.

The design of the ST24C02A and its processing with a highly reliable technology yields to typical endurance better than 1 million cycles and Data Retention greater than 10 years.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

PARAMETER	VALUE	UNITS
Ambient Storage Temperature	- 65 to 150	°C
Input or Output Voltage with respect to ground	- 0.3 to 6.5	V
Lead Temperature (soldering, 10 seconds)	+ 300	°C
ESD Rating	2000	V

OPERATING CONDITIONS

Ambient Operating Temperature		
ST24C02A-1	0 to + 70	°C
ST24C02A-6	- 40 to +85	°C
ST24C02A-3	- 40 to + 125	°C
POWER SUPPLY	4.5 to 5.5	V

D.C. OPERATING CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range
V_{CC} = 5V ±10%

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{CC}	Power Supply Current			2	mA	f_{SCL} = 100kHZ
I_{SB}	Standby Current		100		µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND or V_{CC}
I_{LO}	Ouput Leakage Current			10	µA	V_{OUT} = GND or V_{CC}
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 0.7xV_{cc}		.3xV_{cc} V_{cc} + 1.0	V V	
V_{IL} V_{IH}	Input Low Voltage Input High Voltage	- 1.0 V_{cc} - 0.5		+ 0.5 V_{cc} + 1.0	V V	A0, A1, A2 inputs A0, A1, A2 inputs
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

A.C. CHARACTERISTICS ta=-40°C to +125°C according to selected temperature range
V_{CC} = 5V ±10%

SYMBOL		MIN.	TYP.	MAX.	UNITS
f_{SCL}	SCL Clock Frequency	0		100	kHZ
T_I	Noise Suppression Time Constant on SCL, SDA Inputs			100	ns
t_{AA}	SCL Low to SDA Data Valid	0.3		3.5	µs
t_{BUF}	Time the bus must be be free before a new transmission.	4.7			µs
$t_{HD:STA}$	START Condition Hold Time	4.0			µs
t_{LOW}	Clock Low Period	4.7			µs
t_{HIGH}	Clock High Period	4.0			µs
$t_{SU:STA}$	Start Condition Setup Time (For a repeated START condition)	4.7			µs
$t_{HD:DAT}$	DATA IN Hold Time	0			ns
$t_{SU:DAT}$	DATA IN Setup Time	250			ns
t_R	SDA & SCL Rise Time			1	µs
t_F	SDA & SCL Fall Time			300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4.7			µs
t_{DH}	DATA OUT Hold Time	300			ns
t_{WR}	Programming Time (note 1)			10	ms
Endurance	W/E Cycles	1 million Cycles minimum			

NOTE 1 : In multibyte programming mode and only in this mode, if the accessed words are located in two consecutive rows the maximum programming time will be extended to two times t_{WR}.

FIGURE 1 : BUS TIMING

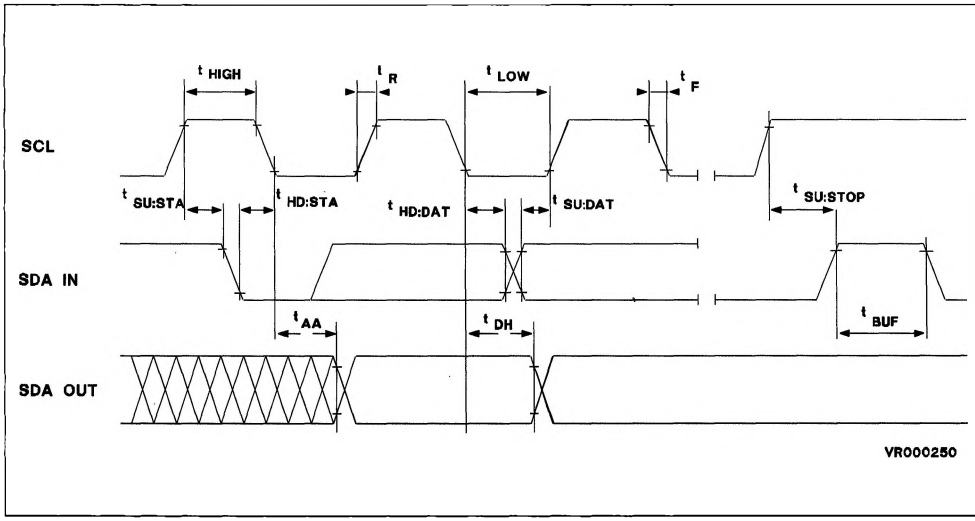
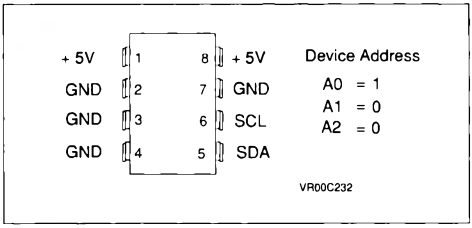


FIGURE 2 : TYPICAL INTERFACE



PIN DESCRIPTION

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into or out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into or out of the device. It is an open drain output that may be wired with any open drain or open collector outputs to formed the system SDA bus.

ADDRESSES (A0,A1,A2)

These three addresses inputs are used to set the least significant bits of the seven bit slave address.These inputs can be used static or seven. When used statically they must be tied to V_{CC} or V_{SS}. When used driven CMOS levels have to applied to the device.

TEST PIN (TEST)

For proper device operation this input must be tied to V_{SS} or V_{CC} According to the voltage on TEST pin up to four or eight bytes may be written in the ST24C02A in a single write operation (see "Write Operation" section.)

DEVICE OPERATION

The ST24C02A supports the I^2C (bidirectional bus oriented) protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and the device being control-led is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations. Therefore, the ST24C02A will be considered as a slave receiver or transmitter in all applications.

DATA TRANSITION

Data transition on the SDA line must only occur when the clock SCL is Low. SDA transitions while SCL is HIGH will be interpreted as START or STOP conditions. (See Fig 1).

START CONDITION

A START condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus. The ST24C02A continuously monitors the SDA and SCL lines for a START and will not respond to any command if this condition has not been met.

STOP CONDITION

A STOP condition is defined by a LOW to HIGH transition of the SDA line while the SCL is at a stable HIGH level. This condition terminates communication between devices and forces the ST24C02A in the standby power mode.

ACKNOWLEDGE

Acknowledge is used to indicate successfull data transfer. The transmitter (master or slave) will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line LOW to indicate it received the 8 bits of data.

DATA TRANSFER

During Data Transfer the ST24C02A samples the SDA line on the leading edge of SCL clock.Therefore,for proper device operation SDA line must be stable during the SCL LOW to HIGH transition.

NOTE

In the I^2C protocol ,the SDA bus must be connected to the positive power supply through a pull-up resistor.

DEVICE ADDRESSING

To start communication between two devices, the bus master must initiate a start instruction sequence; following a START condition the master sends onto the SDA bus an eight bit word correspondind to the address of the device it is addressing.

- The most significant 4 bits of the slave address, therefore the first bits sent onto the bus are the device type identifier. The ST24C02A memory device type is fixed as "1010".

- The next 3 significant bits are used to address a particular device of the previously defined type connected to the bus. The state of the hardwired A0,A1 and A2 pins defines the device address. Up to eight ST24C02A can be connected on the same bus.
- The last bit of the start instruction defines the type of operation to be performed:
  When set to "1" a read operation is selected
  When set to "0" a write operation is selected.

Chip selection is accomplished by setting the three bits of the chip address field to the corresponding levels of A0,A1 and A2 inputs. After a START condition is detected all ST24C02A connected to the bus will compare the slave address being transmitted with their own hardwired address (A0 to A2). After comparison , the selected ST24C02A will acknowledge on the SDA line and will perform the read or write operation according to the state of the R/W bit.

WRITE OPERATION

The standard operation mode is byte write or multibyte programming. If pin 7 is forced to VSS the ST24C02A switches to page mode.

BYTE WRITE

In this mode, following a START condition the master sends a slave address word with the R/W bit set to "0". The ST24C02A will acknowledge this first transmission and waits for a second word : the word address field.This 8 bit address field provides access to any of the 256 words of the memory array. Upon receipt of the word address the ST24C02A slave device will respond with an acknowledge.

At this time, all following words transmitted to the ST24C02A will be considered as Data.

In Byte Write mode the master sends one word which is acknowledged by the ST24C02A .

FIGURE 3 : SLAVE ADDRESS ALLOCATION

	Device type				Device Address			
START	1	0	1	0	A2	A1	A0	R/W
	Slave Address							

Then the master terminates the transfer by generating a STOP condition.

This STOP condition initiates the internal self-timed programming cycle.

While the internal programming cycle is in progress the ST24C02A will not respond to any request from the bus master.

MULTIBYTE PROGRAMMING

The ST24C02A is able to write consecutively up to 4 bytes in the multibyte programming mode.

As in the Byte Write programming mode,the multibyte programming can be started at any specified address and whithout any restriction of any kind.

This multibyte mode is started and performed in the same way as the Byte Write mode; but instead of terminating the write sequence after the first data word is transfered,the master does not generate a STOP condition and up to 3 additional words can be transmitted to the ST24C02A. After receipt of each word,the ST24C02A will respond with an acknowledge.

After the bytes to be written (4 bytes maximun) have been transfered, the master generates a STOP condition which starts the internal self-timed programming cycle.

PAGE WRITE (only available if pin 7 is grounded)

The ST24C02A is able to write up to 8 bytes in a Page Write operation. This mode allows to write 2 to 8 bytes in a single write cycle provided they are all topologically located in the same physical row(five most significant address bits identical.).

This mode is started and performed in the same way as the byte write operation, but instead of terminating the write sequence after the first data word is transfered, the master doesn't generate a STOP condition and can transmit up to seven additional words. After receipt of each word the ST24C02A will respond with an acknowledge.

After receipt of each data word the internal address counter is automatically incremented by one.

Only the three low order address bits are incremented, the high order five bits remain constant.

Therefore, a special attention has to be paid when using this feature in order to avoid any scrambling or over writing.

If more than 8 words are transmitted the address counter will "roll-over" and the previously written

data will be overwritten. As in byte write operation the master terminates the transfer by generating a stop condition that triggers the internal programming cycle. All inputs are disabled until completion of the internal write cycle.

READ OPERATION

Read operations are initiated in the same manner as the write operation with the exception that the R/W bit following the slave address in the start instruction is set to a logical "1". Three read operation modes are available:

. current address read
. random read
. sequential read

CURRENT ADDRESS READ

The ST24C02A has an internal address counter that points the address of the last word accessed incremented by one. Therefore if the last access (either read or write) was to address n, the next current read operation will access data from address n+1. To initiate this read mode the master generates a start instruction (START condition followed by the eight bit slave address word) with the R/W bit set to one. The ST24C02A will respond with an acknowledge and transmit the 8 bits of data. To terminate the transfer the master MUST not acknowledge the transfer but DOES generate a STOP condition.

RANDOM READ

The random read mode allows the master to access any memory location. In order to load into the device the word address the master must first performed a "dummy" write sequence.(START, slave address ,R/W bit set to "0",followed by the word address to be read). After the word address has been acknowledged,the master immediately reissues a START instruction whith the R/W bit set to "1". The ST24C02A will acknowledge the transfer and output the 8 bits of the addressed word. As in current address read to terminate the transfer the master MUST not acknowledge the transfer but DOES generate a STOP condition.

SEQUENTIAL READ

This mode can be initiated with either a current address read or random read. The first word read out of the memory is transmitted in the same way as in both previous modes,however the master must now acknowledge the transfer indicating it requires more data. The ST24C02A will output a string of eight bits for each acknowledge it received. As in the other read modes to terminate the transfer the master MUST not acknowledge the last transfer but DOES generate a STOP condition.

The data output is sequential;data from address n followed by data from address n+1. The internal address counter is automaticaly incremented allowing the entire content of the 256 word memory to be serially read in a single read operation. If more than 256 words are read the counter will "roll-over" and the ST24C02A will continue to output data from the memory.

SDA BUS IN READ MODE

In all read modes the ST24C02A is waiting for an acknowledge (SDA line low) on the 9th clock pulse of a data transfer. If an acknowledge is not detected,the ST24C02A terminates the data transfer and switches to a "receiver" state.

TIMING DIAGRAMS

FIGURE 4 : BYTE WRITE

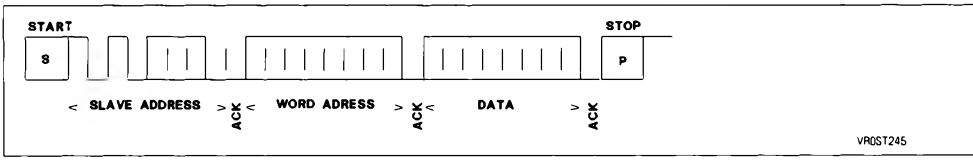


FIGURE 5 : PAGE WRITE

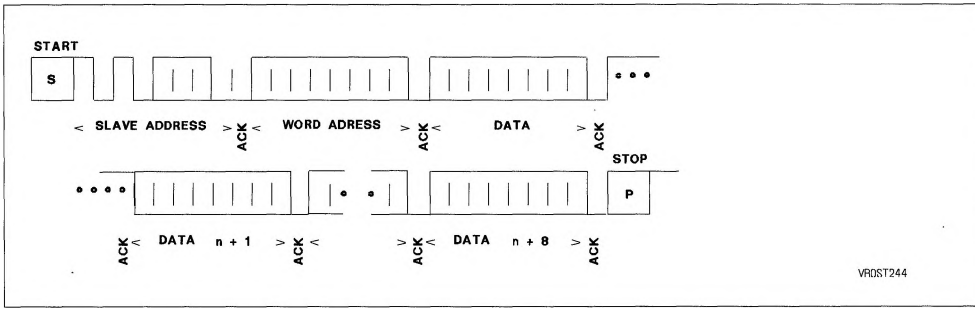


FIGURE 6 : CURRENT ADDRESS READ

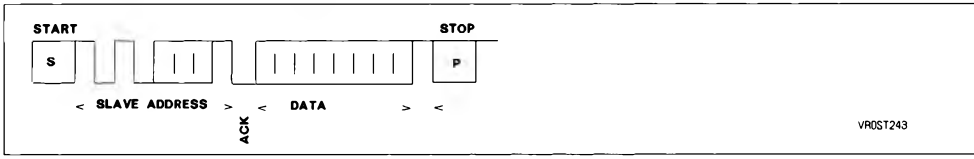


FIGURE 7 : RANDOM ADDRESS READ

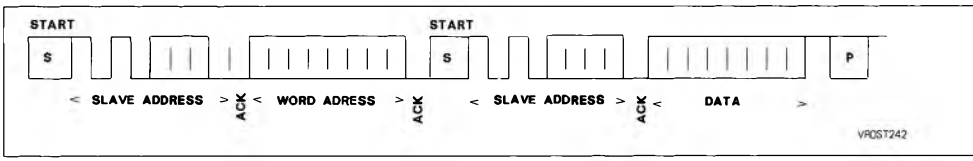
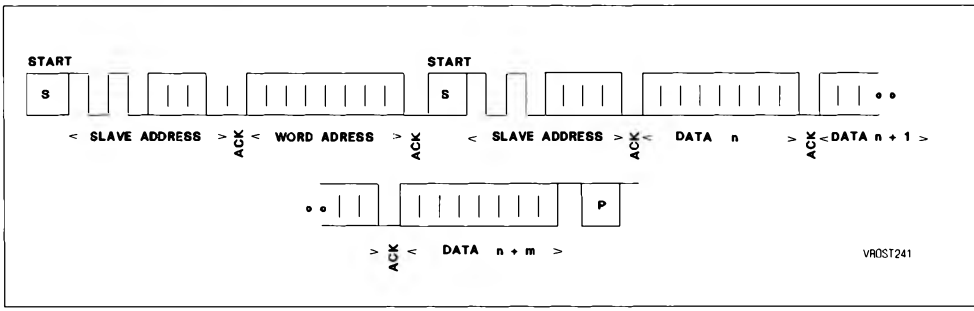


FIGURE 8 : SEQUENTIAL READ

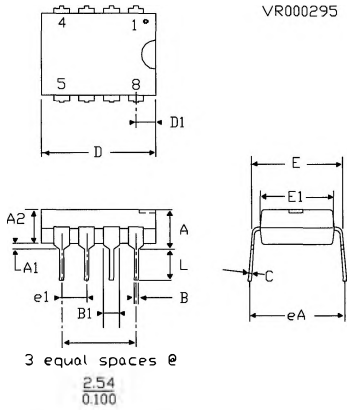


ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	SUPPLY VOLTAGE
ST24C02AB1	Dual-in-line	0°C to 70°C	4.5V to 5.5V
ST24C02AM1	SO 8		
ST24C02AB6	Dual-in-line	-40°C to 85°C	
ST24C02AM6	SO 8		
ST24C02AB3	Dual-in-line	-40°C to 125°C	
ST24C02AM3	SO 8		

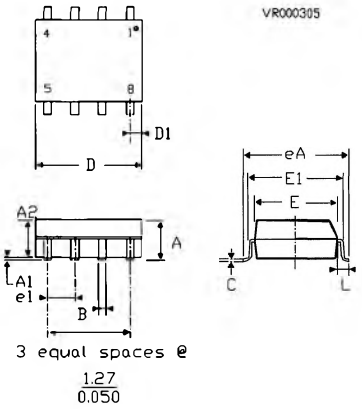
PACKAGE MECHANICAL DATA

PDIP8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050