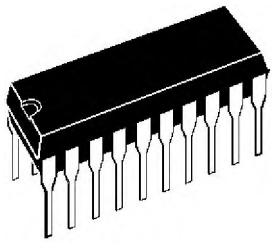
SGS-THOMSON MICROELECTRONICS

ST62T09

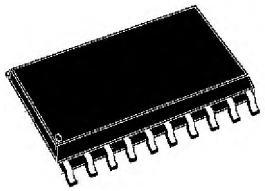
8-BIT OTP MCUs WITH A/D CONVERTER

PRELIMINARY DATA

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait and Stop Modes
- 4 Interrupt Vectors
- Look-up Table capability in OTP
- Data OTP: User selectable size (in program OTP)
- Data RAM: 64 bytes
- 12 I/O pins, fully programmable as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull output
  - Analog Input
- 4 I/O lines can sink up to 20mA to drive LEDs or TRIACs directly
- 8-bit Timer/Counter with 7-bit programmable prescaler
- Digital Watchdog
- 8-bit A/D Converter with 4 analog inputs
- On-chip Clock oscillator can be driven by Quartz crystal or Ceramic resonator
- Power-on Reset
- One external Non-Maskable Interrupt
- ST626x-EMU Emulation and Development System (connects to an MS-DOS PC via an RS232 serial line).



PDIP20



PSO20

(See end of Datasheet for Ordering Information)

DEVICE SUMMARY

DEVICE	OTP (Bytes)	I/O Pins
ST62T09	1036	12

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1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST62T09 device is a low cost member of the ST62xx 8-bit HCMOS family of microcontrollers, which is targeted at low to medium complexity applications. All ST62xx devices are based on a building block approach: a common core is surrounded by a number of on-chip peripherals.

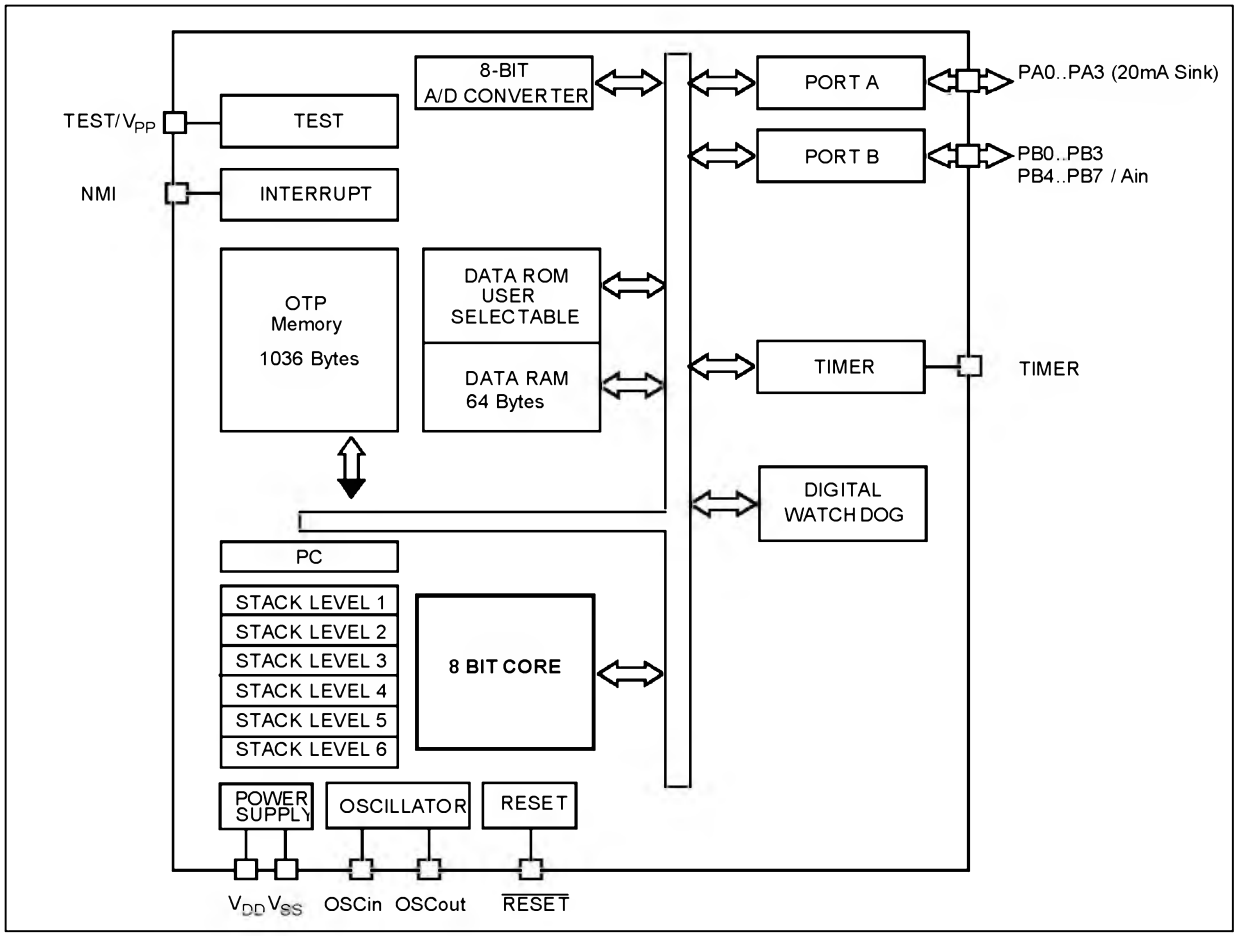
OTP devices are functionally identical to their ROM counterparts; in addition, the ROM based versions offer the following additional features: RC Oscillator, Oscillator Safeguard, external Stop mode control, program code readout protection and an optional internal pullup on the NMI and TIMER pins.

OTP devices offer all the advantages of user programmability at low cost, which make them the ideal choice in a wide range of applications where frequent code changes, multiple code versions or last minute programmability are required.

The ST62E20 (4K EPROM) device may be used to emulate the ST62T09 OTP device, but care should be taken not to exceed the memory size of the T09 device.

These compact low-cost devices feature a Timer comprising an 8-bit counter and a 7-bit programmable prescaler, an 8-bit A/D Converter with 4 analog inputs and a Digital Watchdog timer, making them well suited for a wide range of automotive, appliance and industrial applications.

Figure 1. Block Diagram



1.2 PIN DESCRIPTIONS

V_{DD} and V_{SS}. Power is supplied to the MCU via these two pins. V_{DD} is the power connection and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected to the on-chip oscillator circuit. A quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins. The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active-low $\overline{\text{RESET}}$ pin is used to restart the microcontroller.

TEST/V_{PP}. The TEST must be held at V_{SS} for normal operation. If TEST pin is connected to a +12.5V level during the reset phase, the EPROM/OTP programming Mode is entered.

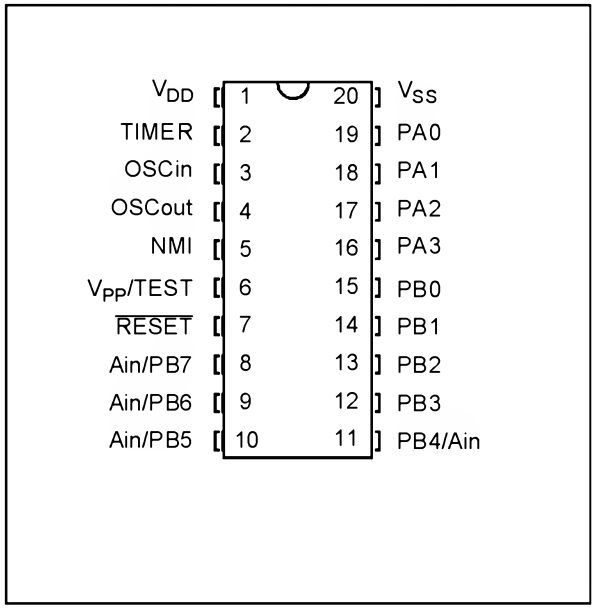
NMI. The NMI pin provides the capability for asynchronous interruption, by applying an external non maskable interrupt to the MCU. The NMI input is falling edge sensitive. A pull-up device must be provided externally on OTP and EPROM devices.

TIMER. This is the timer I/O pin. In input mode it is connected to the prescaler and acts as external timer clock input or as control gate input for the internal timer clock. In output mode the timer pin outputs the data bit when a time-out occurs. A pull-up device must be provided externally on OTP and EPROM devices.

PA0-PA3. These 4 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs. **PA0-PA3** can also sink 20mA for direct LED driving.

PB0-PB7. These 8 lines are organized as one I/O port (B). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter.

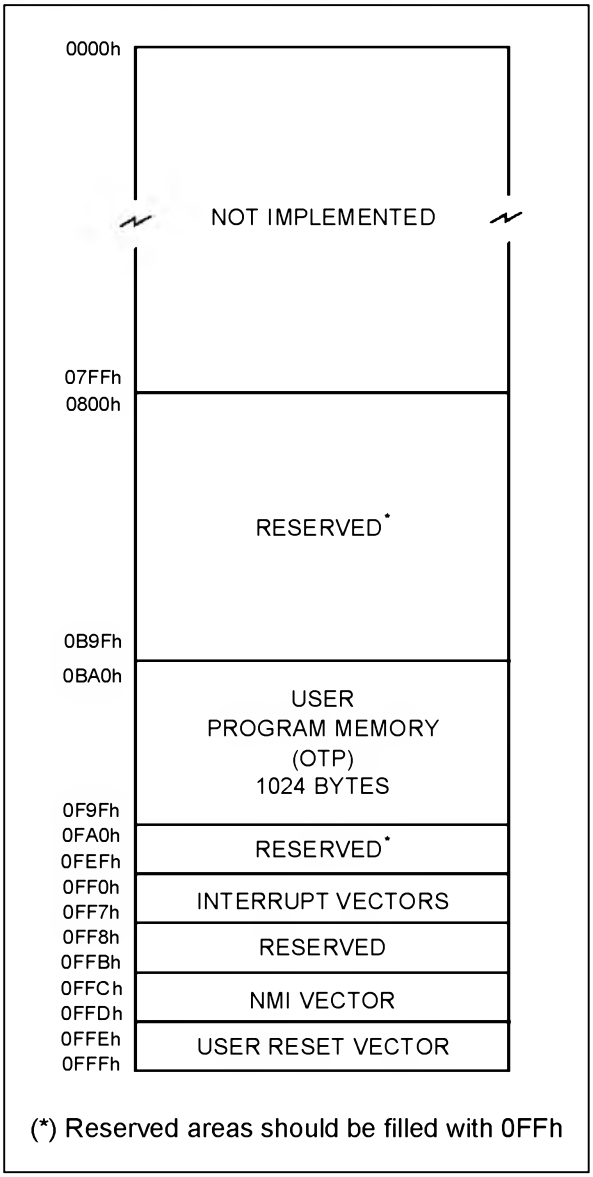
Figure 1. ST62T09 Pin Configuration



1.3 MEMORY MAP

1.3.1 Program Memory Map

Figure 2. ST62T09 Program Memory Map



(*) Reserved areas should be filled with 0FFh

1.3.2 Data Space

Data Space accommodates all the data necessary for processing the user program. This space comprises the RAM resource, the processor core and peripheral registers, as well as read-only data such as constants and look-up tables in OTP.

The Data Space is fully described and illustrated on page 18.

1.4 PARTICULARITIES OF OTP DEVICES

OTP and EPROM devices are identical save for the package which, in the EPROM device, is fitted with a transparent window to allow erasure of memory contents by exposure to UV light.

Both OTP and EPROM parts may be programmed using programming equipment approved by SGS-THOMSON.

1.4.1 OTP Programming

Programming mode is selected by applying a 12.5V voltage to the V_{PP}/TEST pin during reset. Programming of OTP and EPROM parts is fully described in the EPROM Programming Board User Manual.

1.4.2 Eprom Erasure

Thanks to the transparent window present in the EPROM package, its memory contents may be erased by exposure to UV light.

Erasure begins when the device is exposed to light with a wavelength shorter than 4000Å. It should be noted that sunlight, as well as some types of artificial light, includes wavelengths in the 3000-4000Å range which, on prolonged exposure, can cause erasure of memory contents. It is thus recommended that EPROM devices be fitted with an opaque label over the window area in order to prevent unintentional erasure.

The recommended erasure procedure for EPROM devices consists of exposure to short wave UV light having a wavelength of 2537Å. The minimum recommended integrated dose (intensity x exposure time) for complete erasure is 15Wsec/cm^2. This is equivalent to an erasure time of 15-20 minutes using a UV source having an intensity of 12mW/cm^2 at a distance of 25mm (1 inch) from the device window.

2 CENTRAL PROCESSING UNIT

2.1 INTRODUCTION

The CPU Core may be thought of as an independent central processor communicating with on-chip I/O, memory and peripherals. For further details refer to page 14.

2.2 CPU REGISTERS

The CPU Core features six registers and three pairs of flags available to the programmer. For a detailed description refer to page 20.

3 CLOCKS, RESET, INTERRUPTS AND POWER SAVING MODES

3.1 CLOCK SYSTEM

The Oscillator may be driven by an external clock, or by a crystal or ceramic resonator. ROM devices also offer RC oscillator and Oscillator Safeguard features. For a complete description refer to page 22.

3.2 RESETS

The MCU can be reset in three ways: by the external Reset input being pulled low, by the Power-on Reset circuit, or by the Digital Watchdog timing out. For further details refer to page 26.

3.3 DIGITAL WATCHDOG

The Digital Watchdog can be used to provide controlled recovery from software upsets. Software and Hardware enabled Watchdog options are available in order to achieve optimum trade-off between power consumption and noise immunity. For a complete description and a selection guide refer to page 29.

3.4 INTERRUPTS

The CPU can manage four Maskable and one Non-Maskable Interrupt source. Each source is associated with a specific Interrupt Vector. An internal pullup option on the NMI pin is available on ROM devices. For a complete description refer to page 33.

3.5 POWER SAVING MODES

WAIT mode reduces electrical consumption during idle periods, while STOP mode achieves the lowest power consumption by stopping all CPU activity. For a complete description refer to page 37.

3.6 I/O PORTS

Input/Output lines may be individually programmed as one of a number of different configurations. For further details refer to page 39.

3.7 TIMER

The on-chip Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, giving a maximum count of 2^{15}. For a complete description refer to page 43.

3.8 A/D CONVERTER (ADC)

The 8-bit on-chip ADC features multiplexed analog inputs, as alternate I/O functions. Conversion is by successive approximations, with a typical conversion time of 70us, at 8MHz oscillator frequency. For a complete description refer to page 46.

4 SOFTWARE

4.1 ST6 ARCHITECTURE

The ST6 architecture has been designed to exploit the hardware in the most efficient way possible, while keeping byte usage to a minimum. For further details refer to page 48.

4.2 ADDRESSING MODES

The ST6 core offers nine addressing modes: Immediate, Direct, Short Direct, Extended, Program Counter Relative, Bit Direct, Bit Test & Branch, Indirect, and Inherent. For a complete description of the available addressing modes, refer to page 48.

4.3 INSTRUCTION SET

The ST6 core offers a set of 40 basic instructions which, when combined with nine addressing modes, yield 244 usable opcodes; these may be subdivided into six types: load/store, arithmetic/logic, conditional branch, control, jump/call, and bit manipulation. For further details refer to page 49.

5 ELECTRICAL CHARACTERISTICS

5.1 ABSOLUTE MAXIMUM RATINGS

This product contains devices designed to protect the inputs against damage due to high static voltages; however, it is advisable to take normal precautions to avoid applying voltages higher than the specified maximum ratings.

For proper operation, it is recommended that V_I and V_O be higher than V_{SS} and lower than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriate logic voltage level (V_{DD} or V_{SS}).

Power Considerations.The average chip-junction temperature, T_j, in degrees Celsius can be obtained from:

$$T_j = T_A + P_D \times R_{thJA}$$

Where:

T_A = Ambient Temperature.

R_{thJA} =Package thermal resistance (junction-to ambient).

$P_D = P_{int} + P_{port}$

$P_{int} = I_{DD} \times V_{DD}$ (chip internal power).

P_{port} =Port power dissipation (to be determined by the user)

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3(1)	V
V_{PP}	OTP/EPROM Programming Voltage	13	V
I_O	Current Drain per Pin Excluding VDD, VSS	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, VDD = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
$\|I_{DD}\|$	Total Current into V_{DD} (source)	50(2)	mA
$\|I_{SS}\|$	Total Current out of V_{SS} (sink)	50(2)	mA
T_j	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes:

Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

(1) Within these limits, clamping diodes are non-conducting. Voltages outside these limits are authorised provided injection current is kept within the specification.

(2) The total current through ports A and B combined may not exceed 50mA. If the application is designed with care and observing the limits stated above, total current may reach 50mA.

5.2 THERMAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
R_{thJA}	Thermal Resistance (junction to ambient)	PDIP20			60	°C/W
		PSO20			80	

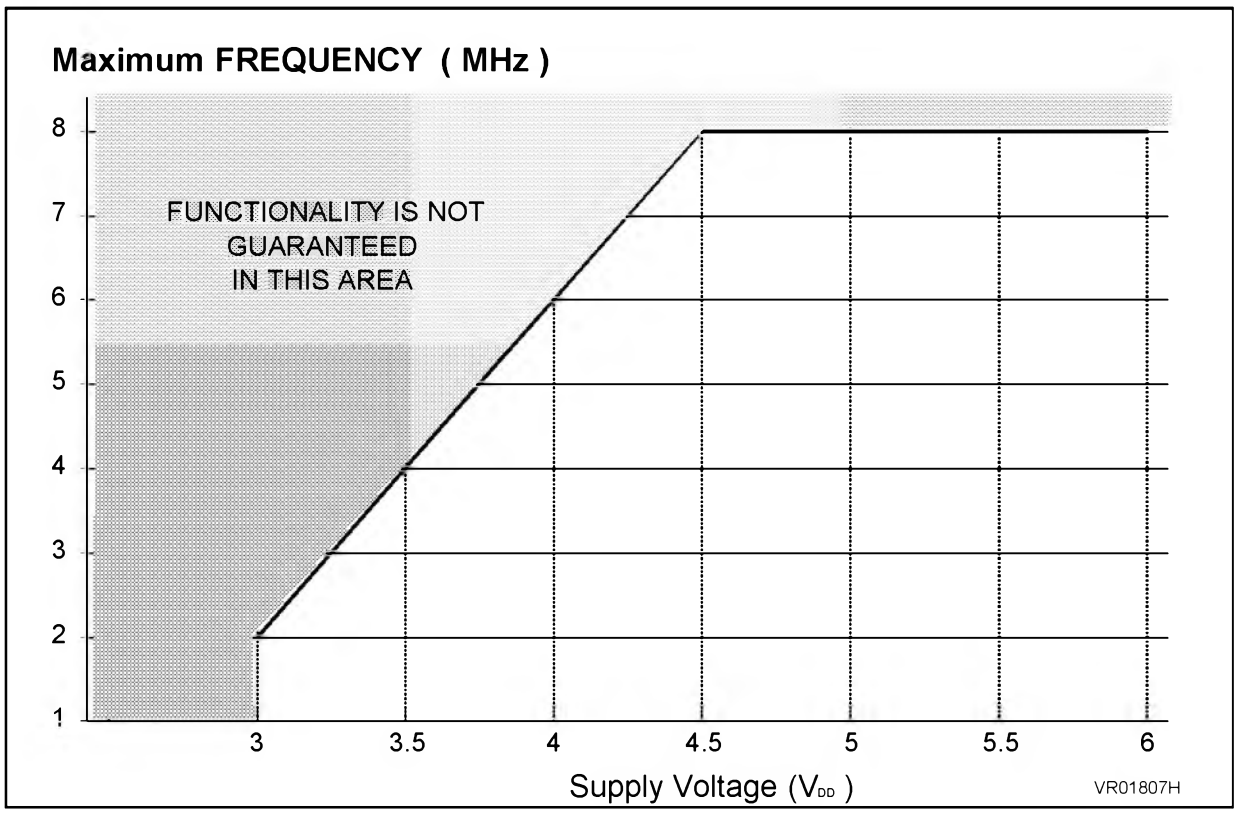
5.3 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage		3.0V		6.0V	V
V_{PP}	Programming Voltage		12	12.5	13	V
I_{INJ+}	Pin Injection Current (positive) Digital Input Analog Inputs	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes:

If a total current of +1mA is flowing into a single analog channel, or if the total current flowing into all the analog inputs is 1mA, all resulting A/D conversions will be shifted by + 1 LSB. If a total positive current is flowing into a single analog channel, or if the total current flowing into all analog inputs is 5mA, all the resulting conversions are shifted by + 2 LSB.

Figure 2. Maximum Operating FREQUENCY (F_{MAX}) Versus SUPPLY VOLTAGE (V_{DD})

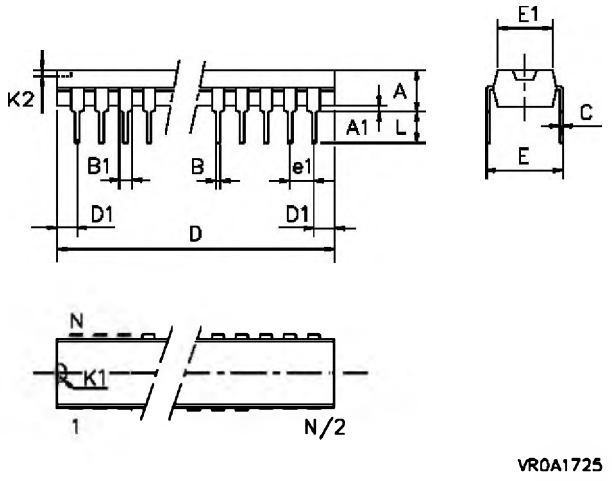


The shaded area is outside the recommended operating range; device functionality is not guaranteed under these conditions.

6 GENERAL INFORMATION

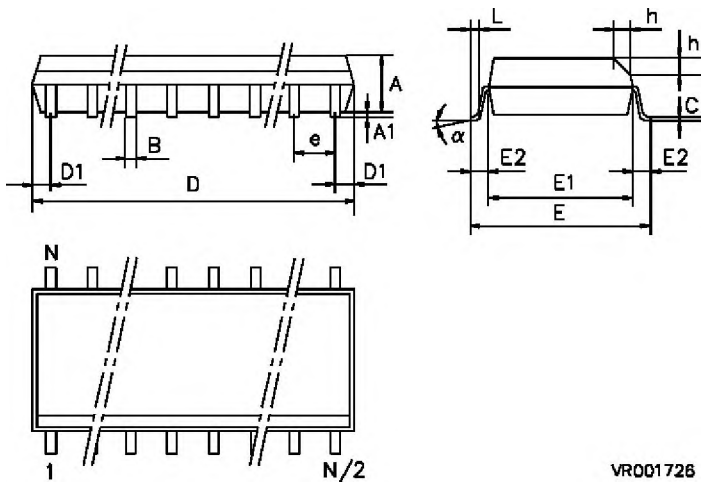
6.1 PACKAGE MECHANICAL DATA

Figure 3. 20-Pin Plastic Dual In-Line Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.93			0.155
A1	0.254			0.010		
A2	-	-	-	-	-	-
B		0.45			0.018	
B1	1.39		1.65	0.055		0.065
C		0.25			0.010	
D			25.4			1.000
e3		22.86			0.900	
E1			7.1			0.280
e		2.54			0.100	
eB		8.5			0.335	
K1	-	-	-	-	-	-
K2	-	-	-	-	-	-
L		3.3			0.130	
	Number of Pins					
N	20					

Figure 4. 20-Pin Plastic Small Outline Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
D1	-	-	-	-	-	-
E	10.00		10.65	0.394		0.419
E1	7.40		7.60	0.291		0.299
E2	-	-	-	-	-	-
e		1.27			0.050	
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
∝	0°		8°			
	Number of Pins					
N	20					

Table 1. OTP Device Sales Types

Sales Type	I/O Pins	Option	Temperature range	Package
ST62T09B6/HWD	12	Hardware Watchdog	-40°C TO +85°C	PDIP20
ST62T09B6/SWD	12	Software Watchdog		
ST62T09M6/HWD	12	Hardware Watchdog		PSO20
ST62T09M6/SWD	12	Software Watchdog		