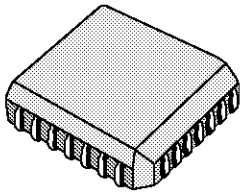
SGS-THOMSON MICROELECTRONICS

ST7537HS1

HOME AUTOMATION MODEM

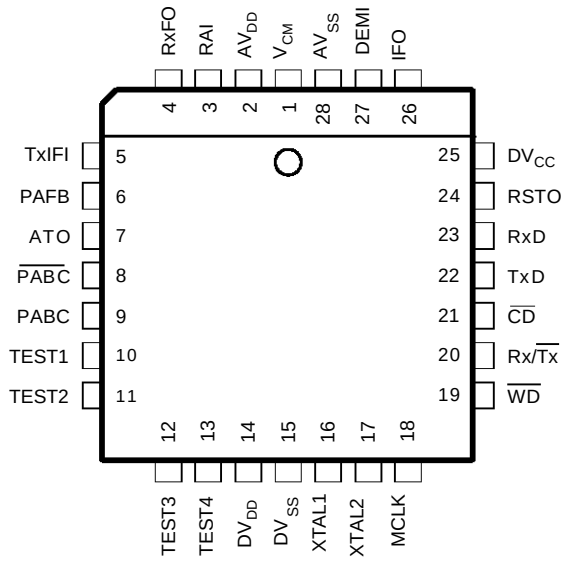
- HALF DUPLEX ASYNCHRONOUS 2400bps FSK MODEM
- Tx CARRIER FREQUENCY SYNTHESIZED FROM EXTERNAL CRYSTAL
- LOW DISTORTION Tx SIGNAL
- Rx SENSITIVITY BETTER THAN 1mV$_{RMS}$
- CARRIER DETECTION
- WATCH-DOG INPUT
- RESET AND MASTER CLOCK OUTPUTS FOR MICROCONTROLLER
- POWER AMPLIFIER BIAS CURRENT CONTROL (HIGH IMPEDANCE IN Rx MODE)
- SIMPLE AND ECONOMICAL APPLICATION SCHEMATICS
- COMPATIBLE WITH CENELEC EN 50065-1 AND FCC SPECIFICATION
- CARRIER DETECT CLAMPING ON RxD PROGRAMMABLE (ALLOWING DEMODULATION ON VERY LOW RECEIVE LEVEL, 1mV$_{RMS}$ TYPICALLY)



PLCC28
(Plastic Chip Carrier)

ORDER CODE : ST7537HS1

PIN CONNECTIONS



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DESCRIPTION

The ST7537HS1 is a half duplex asynchronous FSK MODEM designed for home automation communication on the domestic electric mains which complies with the EN 50065-1 CENELEC standard.

It mainly operates from a 10V power supply and a 5V power supply for the microcontroller digital interface.

It is interfaced to the power line by an external driver, and a transformer (see Application Schematic Diagram). Its data transmission rate is 2400 bps and its carrier frequency is 132.45kHz.

PIN DESCRIPTION

Pin Name	Pin Number	Pin Type	Description
V_{CM}	1	Analog	Common Mode Voltage
AV_{DD}	2	Supply	Analog Power Supply : 10V ±5 %
RAI	3	Analog	Receive Analog Input
RxFO	4	Analog	Receive Filter Output
TxIFI	5	Analog	Transmit and Intermediate Frequency Filters Test Input (mode TEST3)
PAFB	6	Analog	Power Amplifier Feed-back Input
ATO	7	Analog	Analog Transmit Output
$\overline{PABC}$	8	Digital (10V)	Power Amplifier Bias Current Control Complementary Output
PABC	9	Digital (10V)	Power Amplifier Bias Current Control Output
TEST1	10	Digital	Tx to Rx Automatic Mode Switching Control Input
TEST2	11	Digital	Automatic Mode Switching Time and Watch-dog Time Reduction Control Input
TEST3	12	Digital	TxIFI Selection Input
TEST4	13	Digital	Undelayed Reset Input
DV_{DD}	14	Supply	Digital Power Supply : 10V ±5%
DV_{SS}	15	Supply	Digital Ground : 0V
XTAL1	16	Digital (10V)	Crystal Oscillator Input
XTAL2	17	Digital (10V)	Crystal Oscillator Output
MCLK	18	Digital	Master Clock Output
$\overline{WD}$	19	Digital	Watch-dog Input
Rx/$\overline{Tx}$	20	Digital	Rx or Tx Mode Selection Input
$\overline{CD}$	21	Digital	Carrier Detect Output
TxD	22	Digital	Transmit Data Input
RxD	23	Digital	Receive Data Output
RSTO	24	Digital	Reset Output
DV_{CC}	25	Supply	Digital Buffers Supply Voltage : 5V ±5 %
IFO	26	Analog	Intermediate Frequency Filter Output
DEMI	27	Analog	Demodulator Input
AV_{SS}	28	Supply	Analog Ground : 0V

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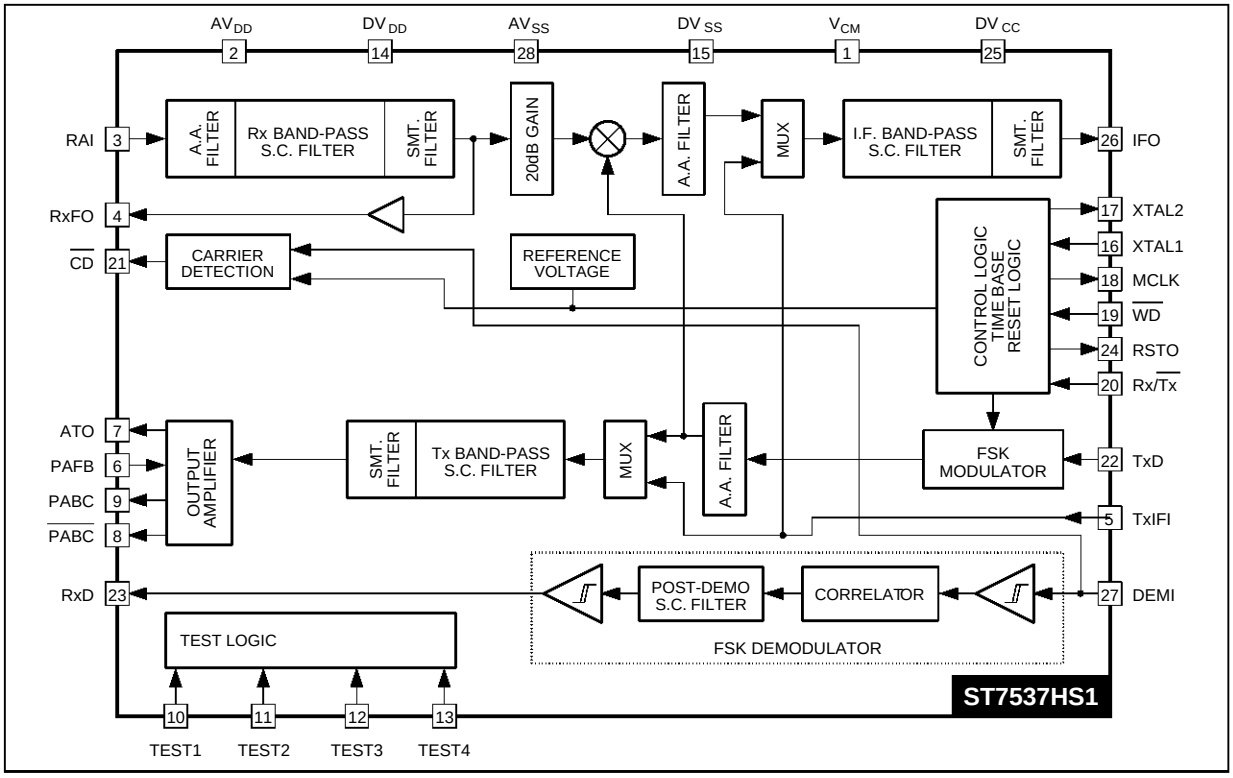
BLOCK DIAGRAM



TRANSMIT SECTION

The transmit mode is set when Rx/$\overline{Tx}$ = 0, if Rx/$\overline{Tx}$ is held at 0 longer than 1 second, then the device switches automatically in the Rx mode. A new activation of the Tx mode requires Rx/Tx to be returned to 1 for a minimum 2 microsecond period before being set to 0.

The Transmit Data (TxD) enter asynchronously the FSK modulator with a nominal intra-message data rate of 2400 bps.

The basic transmit frequencies are :
- f(TxD=0) = 133.05kHz
- f(TxD=1) = 131.85kHz

These frequencies are synthesized from a 11.0592MHz crystal oscillator; their precision is the same as the crystal one's (100ppm).

The modulated signal coming out of the FSK modulator is filtered by a switched-capacitor band-pass filter (Tx band-pass) in order to limit the output spectrum and to reduce the level of harmonic components.

The final stage of the Tx path consists of an operational amplifier which needs a feed-back signal (PAFB) from the power amplifier as shown on Application Schematic Diagram.

In Tx mode the Receive Data (RxD) signal is set to 1.

RECEIVE SECTION

The receive section is active when Rx/$\overline{Tx}$ = 1.

The Rx signal is applied on RAI and filtered by a band-pass switched capacitor filter (Rx band-pass) centered on the carrier frequency and whose bandwidth is around 12kHz.

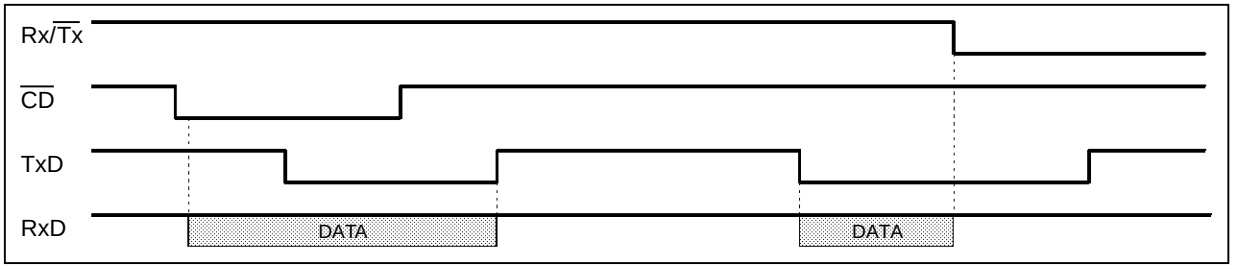
The Rx filter output is amplified by a 20dB gain stage which provides symetrical limitations for large voltage. The resulting signal is down-converted by a mixer which receives a local oscillator synthesized by the FSK modulator block. Finally an intermediate frequency band-pass filter (IF band-pass) whose central frequency is 5.4kHz improves the signal to noise ratio before entering the FSK demodulator.

The coupling of the intermediate frequency filter output (IFO) to the FSK demodulator input (DEMI) is made by an external capacitor C5 (100nF ±10%, 10V) which cancels the Rx path offset voltage.

The RxD output delivers the demodulated signal if the carrier detect ($\overline{CD}$) signal is low and is set to high level when $\overline{CD}$ = 1.

The RxD output can delivers the demodulated signal whatever the level of $\overline{CD}$ (0 or 1) if Rx/$\overline{Tx}$ = 1 and TxD = 0 (see Figure 1).

Figure 1 : Data Timing Chart



ADDITIONAL DIGITAL AND ANALOG FUNCTIONS

Time base

A time base section delivers all the internal clocks from a crystal oscillator (11.0592MHz). The crystal is connected between XTAL1 and XTAL2 pins and needs two external capacitors C3 and C4 (22pF ±10%, 10V) for proper operation.

Reset and watch-dog

The reset output (RSTO) is driven high when the supply voltage is lower than Vrh (typically 7.6V) with an hysteresis Vrh-Vrl (typically 300mV) or when no negative transition occurs on the watch-dog input (WD) for more than 1.5 second (see the timing chart on Figure 2). When a reset occurs RSTO is held high for at least 50ms.

Signal detection

The Carrier Detect output ($\overline{CD}$) is driven low when the input signal amplitude on RAI is greater than V_{CD} for at least T_{CD} (typically 6ms see the timing chart on Figure 3). When the input signal desappears or becomes lower than V_{CD}, $\overline{CD}$ is held low for at least Tcd before returning to a high level. V_{CD} is the carrier detection threshold voltage which is set internally to detect $5mV_{RMS}$ typically.

External power amplifier bias control

Two dedicated digital output (PABC and $\overline{PABC}$) delivering a signal between 0V and 10V are driven low respectively high, when the circuit is set in the receive mode (Rx/$\overline{Tx}$=1) or when the transmit mode time out (1 second) is exceeded; in the same time the output ATO is put in a high impedance state.

TESTING FEATURES

- An additionnal amplifier allows the observation of the Rx band-pass filter output on pin RxFO.
- A direct input to the Tx band-pass filter and to the IF filter (TxIFI) is selected when TEST3 = 1.
- The 1 second normal duration of the Tx to Rx mode automatic switching is reduced to 488µs and the 1.5 second watch-dog time out is reduced to 46.3µs when TEST2 = 1.
- When TEST1 = 1 the Tx to Rx mode automatic switching is desactivated and the functional mode of the circuit is fully controlled by Rx/Tx.
- TEST4 is a reset input which allows an undelayed control of RSTO and of the internal state of the circuit.

POWER SUPPLIES WIRING PRECAUTIONS

The ST7537HS1 has two positive power supply terminals (AV_{DD},DV_{DD}) and two ground terminals (AV_{SS},DV_{SS}) in order to separate internal analog and digital supplies. The analog and digital terminals of each supply pair must be connected together externally for proper operation.

The V_{DD} must be protected against short-circuit for proper operation.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD}/DV_{DD}	Supply Voltage (1)	- 0.3, + 12	V
V_I	Digital Input Voltage	DV_{SS} - 0.3, DV_{DD} + 0.3	V
V_O	Digital Output Voltage (microcontroller interface)	DV_{SS} - 0.3, DV_{CC} + 0.3	V
V_O	Digital Output Voltage (PABC and $\overline{PABC}$)	DV_{SS} - 0.3, DV_{DD} + 0.3	V
I_O	Digital Output Current	- 5, + 5	mA
V_I	Analog Input Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
V_O	Analog Output Voltage	AV_{SS} - 0.3, AV_{DD} + 0.3	V
I_O	Analog Output Current	- 5, + 5	mA
P_D	Power Dissipation	500	mW
T_{oper}	Operating Temperature	0, + 70	^oC
T_{stg}	Storage Temperature	- 55, + 150	^oC

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Notes : 1. The voltages are referenced to AV_{SS} and DV_{SS}.
2. Absolute maximum ratings are values beyond which damage to device may occur. Functional operation under these conditions is not implied.

GENERAL ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \leq T_{amb} \leq 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AV_{DD} DV_{DD}	Supply Voltage		9.5	10	10.5	V
AI_{DD} + DI_{DD}	Supply Current			30		mA
DV_{CC}	Digital Output Supply Voltage		4.75		5.25	V
DI_{CC}	Digital Output Supply Current			1.5		mA
V_{IH}	High Level Input Voltage	Digital Inputs	4.2			V
V_{IL}	Low Level Input Voltage	Digital Inputs			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -100µA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$	 4.9 9.8			 V V
V_{OL}	Low Level Output Voltage	I_{OL} = 100µA • Digital Outputs • Digital Outputs PABC and $\overline{PABC}$			 0.1 0.2	 V V
DC	Duty Cycle	MCLK Output, C_L = 15pF	40		60	%

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TRANSMITTER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \leq T_{amb} \leq 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VTAC	Max Carrier Output AC Voltage	R_L = 5.6kΩ $R_L(AV_{SS})$ = 5.6kΩ R(ATO, PAFB) = 1kΩ	0.8	1.0	1.3	V_{RMS}
HD2	Second Harmonic Distortion			- 50		dB
HD3	Third Harmonic Distortion			- 60		dB
FD	FSK Peak-to-peak Deviation			1200		Hz

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RECEIVER ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \le T_{amb} \le 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input Sensitivity			1	10	mV_{RMS}
V_{IN}	Maximum Input Signal				2	V_{RMS}
R_{IN}	Input Impedance		15			kΩ
GRx	Receive Gain	f = 132.45kHz		20		dB
BER	Bit Error Rate (1)	S/N = 15dB, S = $10mV_{RMS}$, N : white		10^{-5}	10^{-3}	
t_{DEM}	Demodulation Time	Alternate 0 , 1 sequence		3		T bit
V_{CD}	Carrier Detection Level	f = 132.45kHz, sine wave		5	10	mV_{RMS}

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Note 1 : This parameter is guaranteed by correlation

ADDITIONAL DIGITAL AND ANALOG FUNCTIONS ELECTRICAL CHARACTERISTICS

(A/DV_{DD} = 10V, A/DV_{SS} = 0V, DV_{CC} = 5V and $0^oC \le T_{amb} \le 70^oC$, unless otherwise specificied)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RH}	High Level Reset Voltage	See Figure 2		7.9		V
V_{RL}	Low Level Reset Voltage	See Figure 2		7.6		V
t_{RST}	Reset Time	See Figure 2	50			ms
t_{WD}	Watch-dog Pulse Width	See Figure 2	500			ns
t_{WM}	Watch-dog Pulse Period	See Figure 2	800			µs
t_{OUT}	Watch-dog Time Out	See Figure 2			1.5	s
t_{CD}	Carrier Detection Time	See Figure 3	3		6.5	ms

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Figure 2 : Reset and Watch-dog Timing Chart

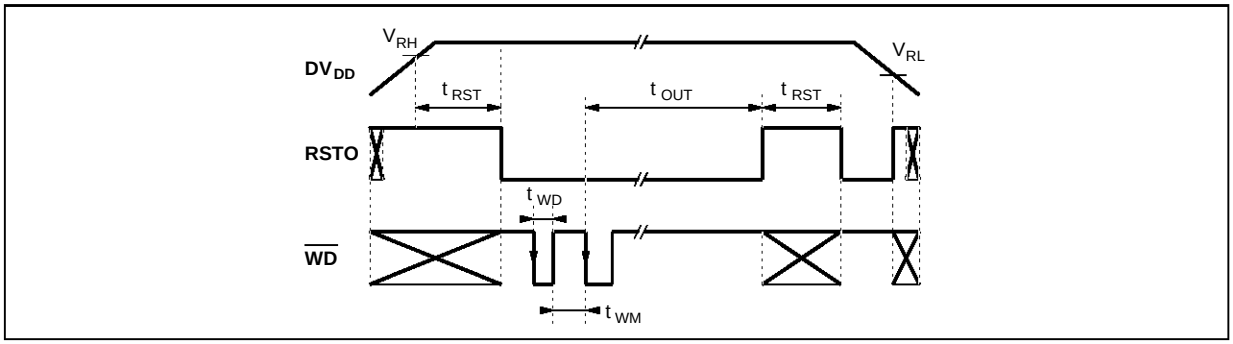

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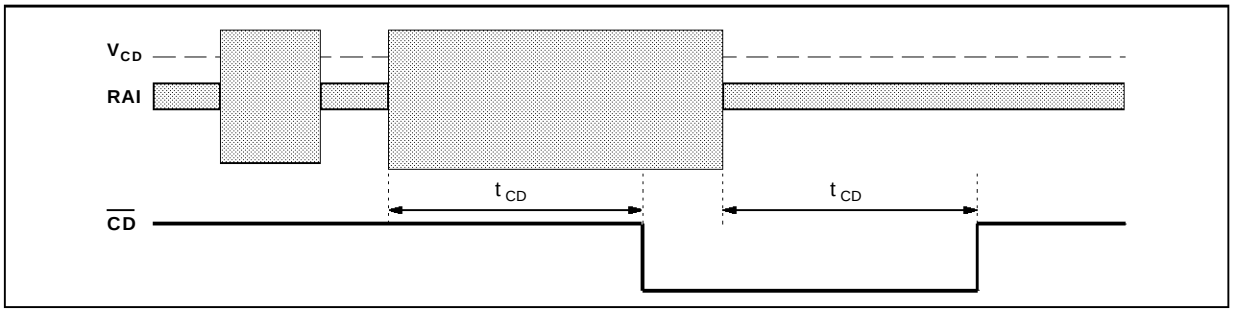
Figure 3 : Carrier Detection Timing Chart



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FILTER TEMPLATES

Receive and Transmit Filter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
92			- 30
126.45	- 5	- 3	- 2
Ref 132.45		0	
138.45	- 5	- 3	- 2
180			- 30

Intermediate FrequencyFilter

Frequency (kHz)	Gain (dB)		
	Min.	Typ.	Max.
2.4			- 35
4.3	- 4	- 3	- 1
Ref 5.4		0	
6.5	- 5	- 3	- 2
11.6			- 35

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APPLICATION SCHEMATIC INFORMATIONS

RESISTORS			CAPACITORS			
R1	180Ω		C1	1µF		Ceramic 50
R2	2.2Ω		C2	470nF		Paper, class X2
R3	2.2Ω		C3 (2)	22pF	10%	Ceramic 10V
R4	2.2Ω		C4 (2)	22pF	10%	Ceramic 10V
R5	2.2Ω		C5	100nF	10%	Ceramic 10V
R6	180Ω		C6	6.8nF	5%	Plastic Film 50V
R7	47kΩ		C7	100nF		Ceramic 10V
R8	1kΩ		C8	2.2µF		
R9	1kΩ	5%	C9	100nF		Ceramic 10V
R11	47kΩ		C10	2.2µF		
INDUCTOR			C11 (1)	100nF		Ceramic 10V
L1	10µH	≅ 1.5Ω	C12 (1)	100nF		Ceramic 10V

TRANSISTORS	TRANSIL
Q1 : 2N2907 Q2 : 2N2222 Q3 : 2N2222 Q4 : 2N2907 Q5 : 2N2907 Q6 : 2N2222	TRL1 : SGS-THOMSON P6KE6V8CP
	TRANSFORMER
	TR1 : TOKO T1002 N
	CRYSTAL
	QTZ1 : 11.0592MHz parallel resonance

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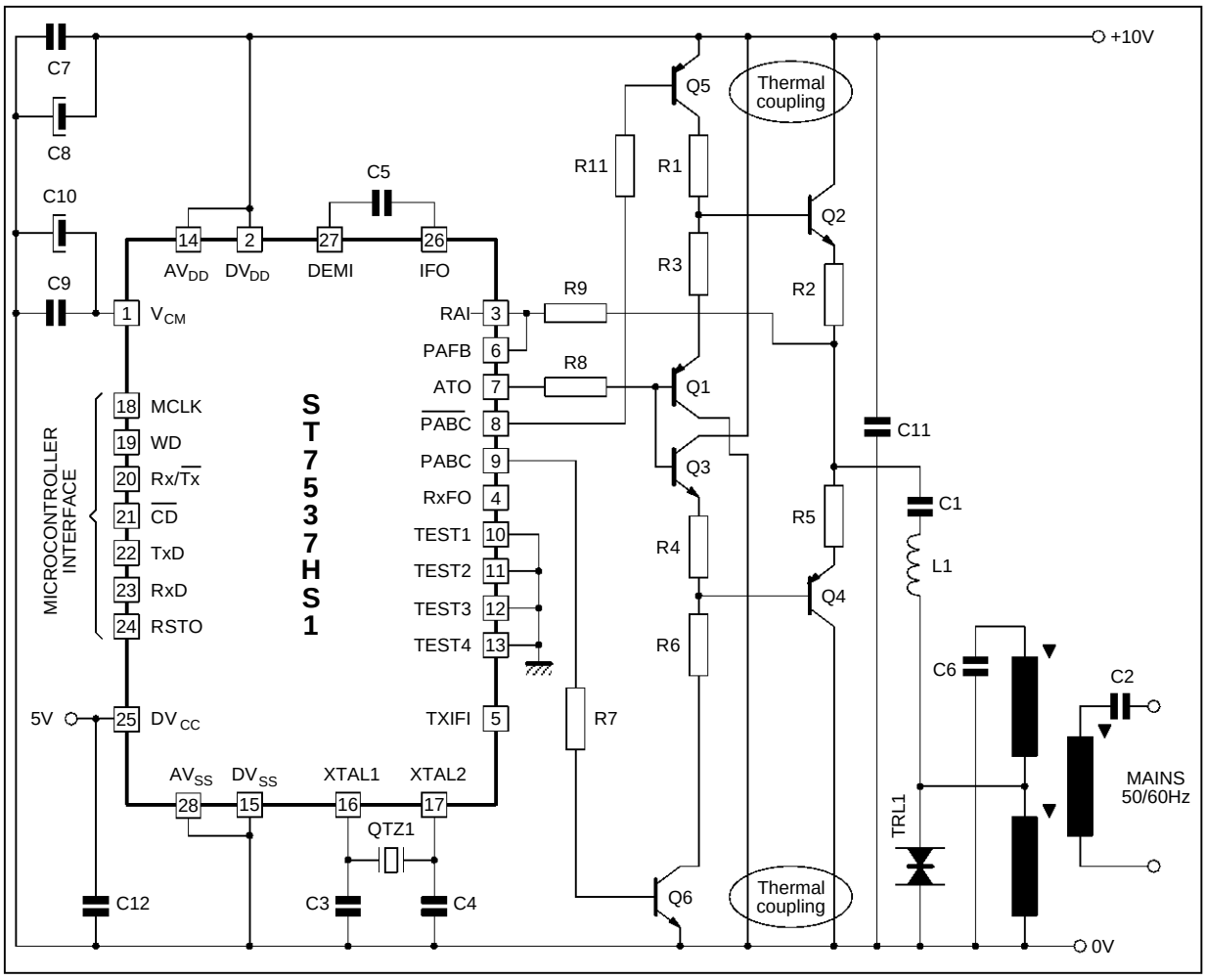
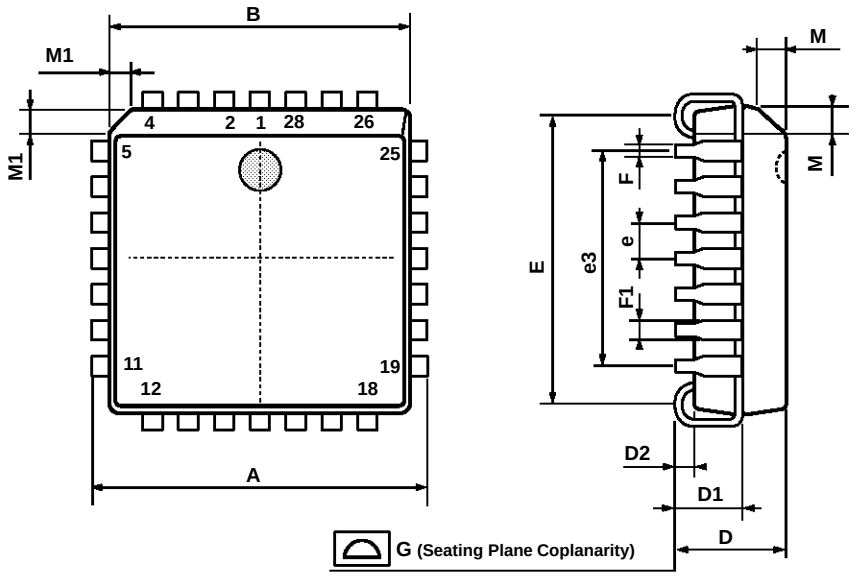
Notes : 1. These capacitors might not be necessary if the overall power supplies decoupling is sufficient.
2. The value of these capacitors depends on the crystal parameters.

APPLICATION SCHEMATIC DIAGRAM



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC CHIP CARRIER



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Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

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SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

ST7537 POWER LINE MODEM APPLICATION

By Joël HULOUX and Laurent HANUS

SUMMARY

I - FOREWORD :

HOME AUTOMATION CONCEPT

Kenneth P. Wacks, consultant to the home automation industry, has written an article clearly defining the concept of home automation. An extract is given below :

"... Over the past six years a new industry called "home automation" has been developing. This industry will create the next generation of consumer appliances. The primary value added by home automation is the integration of products and services for household use. A few small companies are marketing home automation systems. Large companies and institutions are exploring this emerging industry to determine the market potential.

A communication network in the house will provide the infra-structure for linking appliances, sensors, controllers, and control panels inside the house. This has become feasible by tailoring the communications technologies developed for office automation to the home environment.

I.1 - Home Automation Appliances

In home automation, the term "appliances" refers not only to the familiar kitchen, audio/video, and portable appliances, but also to the components of a heating and cooling system, a security system, and lighting features. Home automation covers a broad range of products and services intended for consumer use. These items are expected to share some common attributes, among which are :

- Emphasis on Subsystems :
  Most appliances in houses today are self-contained in metal or plastic cabinets. Each appliance operates independently to the others. Each appliance has a different set of user control.
  Appliances in a home automation environment are able to exchange data. This allows appliances to be grouped into subsystems. Examples range from familiar subsystems, such as security and audio/video systems, to sophisticated lighting controls with preset dimming levels for banks of lights. A future subsystem might permit a washing machine or a dish-washer to request that a water heater preheat water when needed or when the energy cost is lowest.
- Incorporation of Communications Standard :
  Some of the subsystems mentioned already exist. However, the components of each are interconnected using custom-designed technologies and custom wiring. Home automation standards will relieve the manufacturer of the need to invent an ad hoc communications protocol and to provide wiring for data signals.
- Diverse Locations :
  Once communications standards are developed, manufacturers will be able to locate components of appliances outside the cabinet. Control panels could be placed where convenient for the user, not necessarely mounted on the cabinet. Related appliances, such as clothes washer and a clothes dryer, could share a control panel so the knobs and dials are consistent and easier to operate.

I.2 - The Growth of the Industry

Communications technology and standards play important roles in forecasting the home automation industry. However, the development of applications to use these technologies will set the growth rate that simplify routine activities, spark a desire consumers, or save money.

Thus, the growth rate of the home automation industry is ultimately determinated by the actions of appliance manufacturers. Key among these decisions are :

- Adoption of an Emerging Communications Standard :
  The appliance manufacturers will greatly influence the establishment of a particular communications standard. They may even force an amalgamation of standards from among the current contenders.

- Create New Appliances or Appliances Features : The development of standard communications methods can benefit manufacturers and consumers. The design staff would more likely be encouraged and financed to invent appliances that depend on the exchange of data if a communications infra-structure were already in the house..."

II - INTRODUCTION

In the latest generation of home automation systems, appliances can exchange information by transmitting data over the domestic mains wiring. As a result there is no need to install extra control cables and appliances can be connected to the "network" simply by plugging them into the nearest wall socket. Apart from the obvious saving in installation cost, this virtual network also makes modification and enhancement very simple since new devices just have a wall socket to be instantly connected to the network.

What makes these systems feasible is a new dedicated modem integrated circuit, the SGS-THOMSON ST7537 Home Automation Modem IC, developed specifically for this new high volume consumer market as part of a European Community "ESPRIT" project on domestic automation.

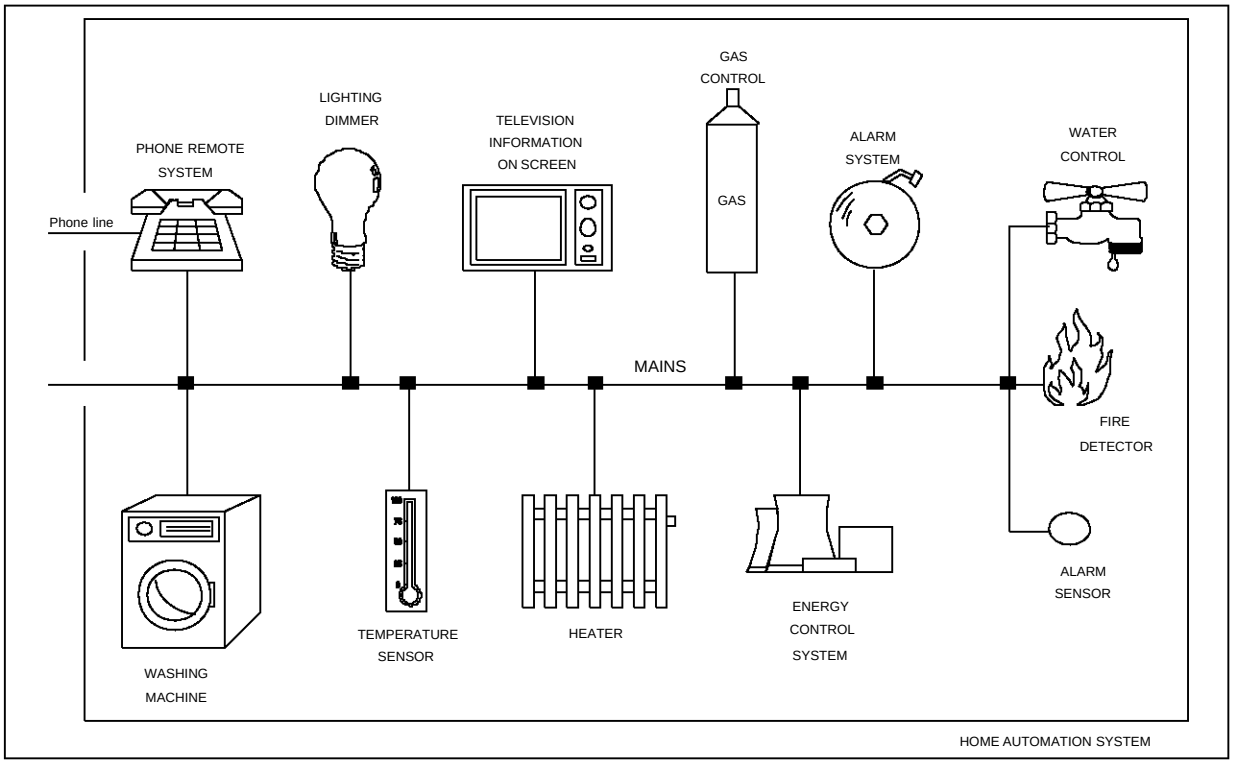
A typical household scenario is shown in Figure 1, where various appliances, sensors, utility controls, a telephone interface and a TV screen display are all connected to the power line using power line modem.

If this automated house catches fire the detector will send a warning message over the line. This will be picked up by the gas control which can cut off the gas supply, by an alarm system that can alert anyone in the house, and even by the telephone interface that can call the emergency services.

The telephone interface also allows the householder to give instructions to appliances from outside. You might, for example, phone home and tell the air conditioner to precool certain rooms at a specified time.

Where there is a limit on energy consumption, or where demand energy pricing is used (now that the technology is available this is likely to be applied extensively in future) various appliances can negociate power requirements through an energy control system. For example, a washing machine can agree with the heating system when it can start a cycle to avoid sudden and unnecessary peaks of demand.

Figure 1 : Typical Household Scenario



III - THE ELECTRICAL NETWORK

Research has been done on the communication properties of the residential power circuit by J.B O'Neal Jr. An extract of his written work is presented below :

"... The primary objective in most residential power line carrier systems is to communicate information from one power outlet in a residence to another. The communication medium, therefore, consists of everything connected on power outlets. This includes house wiring in the walls of the building, appliance wiring, the appliances themselves, the service panel, the triplex wire connecting the service panel to the distribution transformer and the distribution transformer itself. Since distribution transformers usually serve more than one residence, the loads and wiring of all residences connected to the same transformer must be included.

III.1 - Impedance of Power Lines

The most extensive data on this subject has been published by Malack and Engstrom of IBM (Electromagnetic Compatibility Laboratory), who measured the RF impedance of 86 commercial AC power distribution systems in six European countries (see Figure 2).

These measurements show that the impedance of the residential power circuits increases with frequency and is in the range from about 1.5 to 80Ω at 100kHz. It appears that this impedance is determined by two parameters - the loads connected to the network and the impedance of the distribution transformer. The loads at a neighbor's residence can effect this impedance. Wiring seems to have a relatively small effect. The impedance is usually inductive.

For typical resistive loads, signal attenuation is expected to be from 2 to 40dB at 150kHz depending on the distribution transformer used and the size of the loads. Moreover, it may be possible for capacitive loads to resonate with the inductance of the distribution transformer and cause the signal attenuation to vary wildly with frequency.

III.2 - Noise

The principal source of noise is caused by appliances connected to the same transformer secondary to which the power line carrier system is connected. The two primary sources of noise will be triacs used in light dimmers and universal motors. Triacs generate noise synchronous with the 50Hz power signal and this noise appears as harmonics of 50Hz. Universal motors found in mixers, sewing machines, and sanders also create noise, but it is not as strong as light dimmer noise, and not generally synchronous with 50Hz. Furthermore, light dimmers are often left on for long periods of time whereas universal motors are used intermittently. The Figure 3 shows noise sources as well as background noise in a typical residential environment.

Figure 2 : Aggregate European Power Line Impedance (by Malack and Engstrom)

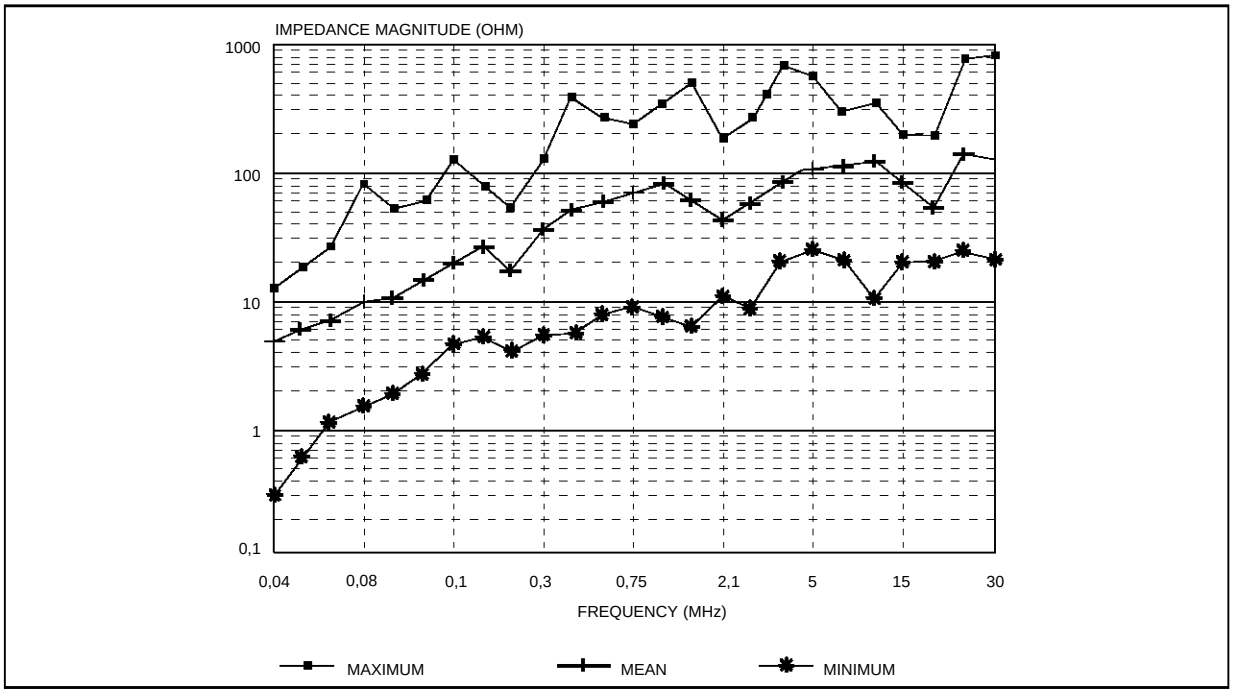
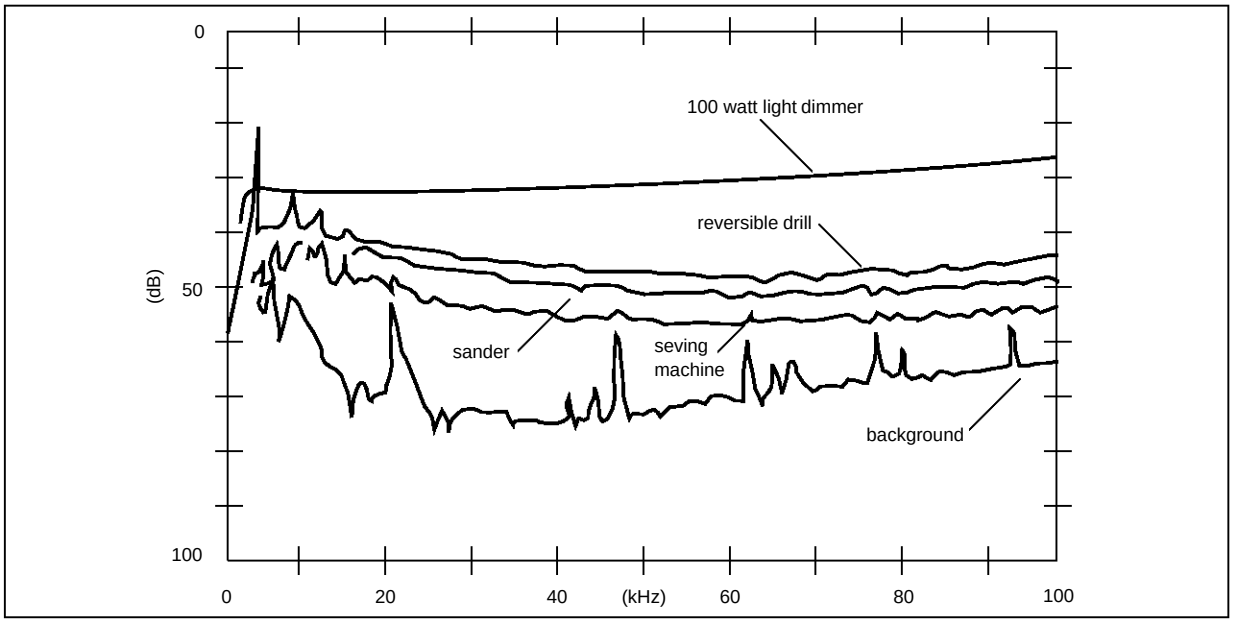


Figure 3 : Voltage spectra for 3 universal motors compared to light dimmers operating into the 60Hz power circuit (by Vines, Trussel, Gale and O'Neal Jr.)



III.3 - Standing Waves

Standing wave effects will begin to occur when the physical dimensions of the communication medium are similar to about one-eight of a wavelenght, which is about 375 and 250 meters at 100 and 150kHz respectively. The length of the communication path on the secondary side of the power distribution system will be determined primarily by the length of the triplex wire connecting the residences to the distribution transformer. Usually, several residences use the same distribution transformer. It would be rare that a linear run of this wiring would exceed 250 meters in length although the total length of branches might occasionally exceed 250 meters. Thus standing wave effects would be rare at frequencies below 150kHz for residential wiring..."

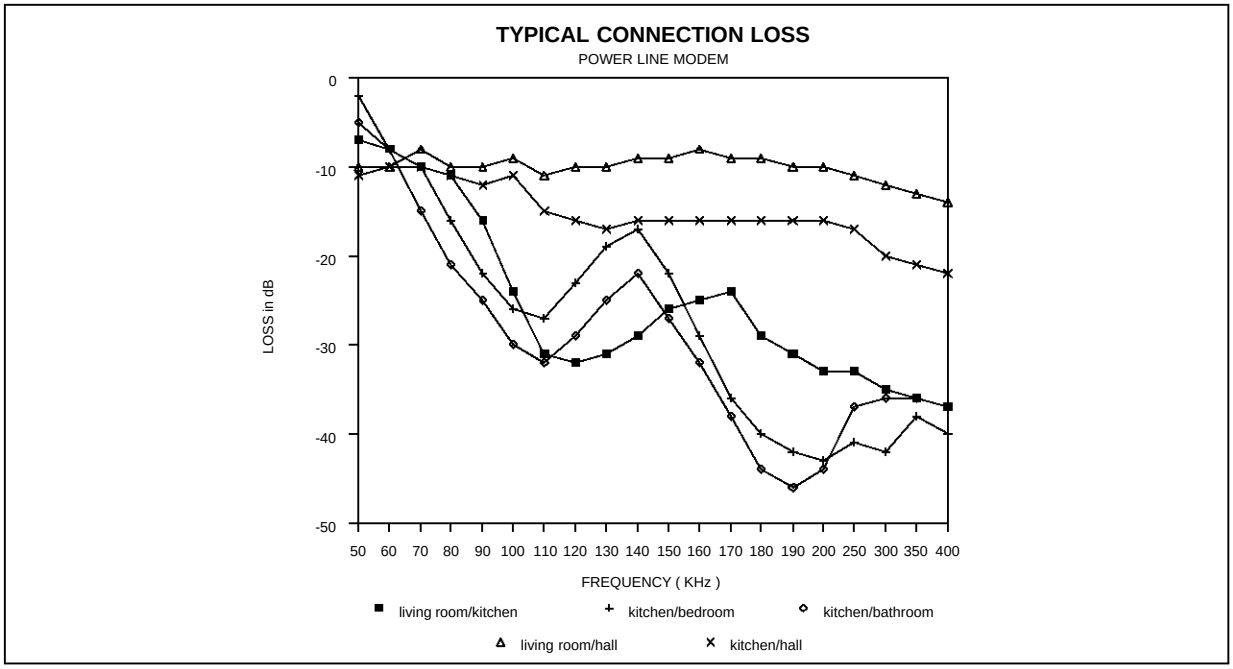
III.4 - Typical Connection Loss (see Figure 4)

We notice two classes of value at a transmit frequency of about 130kHz :

- from 10dB to 15dB : in this case, the transmitter and the receiver are connected to the same branch circuit.
- from 20dB to 30dB : in that case, the transmission path goes from one branch circuit to another through the service panel which induces an additional attenuation of 10dB to 20dB.

Therefore, the transmit range of a home automation system depends on the physical topology of the electric power distribution network inside the building where the system is installed.

Figure 4 : Static Attenuation for Several Paths (by Daniel CHAFFANJON)



IV - ST7537 POWER LINE MODEM

Fabricated in analog CMOS technology, the ST7537 transmits and receives data up to 1200bps in half duplex mode using a carrier frequency of 132.45kHz, complying with Europe's CENELEC EN 50065 standard (which specifies the use of 125kHz to 140kHz carrier frequencies for home automation) and US FCC regulations (which specifies the use of carrier frequencies lower than 450kHz).

Frequency-shift keying is used for transmission, a fundamental design choice that makes it possible to achieve rugged transmission in a very noisy electrical environment at an affordable cost for high volume consumer markets. Among the alternatives, amplitude-shift keying is too susceptible to noise and spread-spectrum, though theoretically more reliable, requires complex and costly circuits. Moreover, field trials in a critical remote utility meter reading application have proven the dependability of the SGS-THOMSON approach.

Included on the chip are all of the functional blocks necessary for the transmission and reception of data over power lines. In addition to this IC the only external components needed are a line driver and a transformer, plus, of course, the microcontroller that prepares and interprets message data.

Transmit data enters the FSK modulator asynchronously with a nominal intra-message data rate of 1200bps. Inside the modulator, the data is transformed into two frequencies (133.05kHz for a "0" and 131.85kHz for a "1"), derived from an inexpensive 11.0592MHz crystal.

The modulated signal from the FSK modulator is filtered by a switched-capacitor bandpass filter (TX bandpass) to limit the output spectrum and to reduce the level of harmonic components. The final stage of the transmit path consists of an operational amplifier which needs a feedback signal from the power amplifier.

In the receive section, the incoming signal is applied at the RAI input (with a typical sensitivity of $1mV_{RMS}$) where it is first filtered by a switched-capacitor bandpass filter with a pass band of around 12kHz, centered on the carrier frequency. The output of the filter is amplified by a 20dB gain stage which provides symetrical limitation for overvoltages. The resulting signal is downconverted by a mixer which receives a local oscillator synthesized by the FSK modulator block.

Finally, an intermediate frequency bandpass filter whose central frequency is 5.4kHz improves the signal-to-noise ratio before entering the FSK demodulator. The coupling of the intermediate frequency filter output to the FSK demodulator input is made by an external capacitor which cancels the receive path offset.

In the ST7537 there are two important additional functions: the carrier detector and the watchdog. Carrier detection is needed because in practically all applications more than two appliances will be connected to the power line. Before attempting to

transmit, an appliance must first check that there is no carrier present, and if there is, it must wait and retry later.

The watchdog function is provided to ensure that the modem's control micro is functioning correctly. Software in the micro must include instructions that send a pulse to the watchdog input of the ST7537 at least once every 1.5s. If no negative transition is observed at this input for 1.5s a reset signal is generated to restart the micro. This watchdog monitor scheme ensures that any disruption caused by glitches are quickly corrected.

V - DEMOBOARD FEATURES

Power line interface

The power line interface has been designed in order to follow the CENELEC EN 50065-1 and US FCC specification. It has to amplify and filter the output signal of the ST7537.

Test pin

It is possible to program the different test modes of the ST7537 with the switches SW1, SW2, SW3 and SW4 corresponding to TEST1, TEST2, TEST3 and TEST4. The most important test mode is TEST1 which allows continuous transmission.

RS232C interface

On the application board, there is an RS232C interface allowing you to debug your system. This interface is connected to the ST7537 by four switches SW5, SW6, SW7 and SW8.

Remark : It is mandatory to provide the watchdog clock to the ST7537.

Wrapping area

You can wire your application and do its debug by connecting relevant digital signals to SW5, SW6, SW7 and SW8 (pin not used) and watchdog, master clock and RSTO.

VI - HARDWARE DESCRIPTION

VI.1 - About CENELEC Specifications

The CENELEC specifications are given for an imaginary network (50Ω/ 50µH + 5Ω) simulating the power line. This network looks like a 54Ω impedance at a transmit frequency of 132.45kHz. The transmitted signal is measured in relation to a reference of this network (see Annexe B). With this configuration, some of the specifications are :

- maximum output level : 116dBµV
- harmonics level of less than 46dBµV mean.

In this chapter, the transmitted signal is measured between the phase and the neutral of the simulated power line. Then, the measured voltages are twice the ones measured with CENELEC test configuration. Thus, it is necessary to add 6dBµV to the specifications given above :

- maximum output level : 122dBµV
- harmonics level of less than 52dBµV mean.

Henceforth, these values will be used .

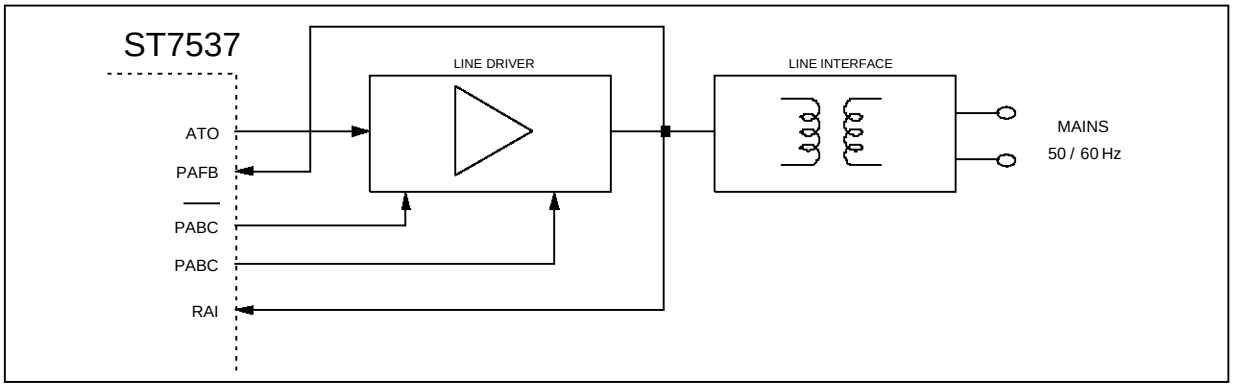
VI.2 - Power Line Interface

The power line interface connects the ST7537 to the power lines and meets the CENELEC and FCC specifications. It has the following functions :

- in transmit mode : to amplify and filter the transmit signal (ATO) from the ST7537
- in receive mode : to provide received signal from powerlines to the receive input (RAI) of the ST7537
- protection against spikes and overvoltages.

It is composed of a line driver and a line interface as it is shown in Figure 5.

Figure 5 : Power Line Interface Description



In transmit mode, the power line interface has to be able to drive, via the line interface, power lines with impedances from 1 to 100Ω. The line interface is not only used to put signals on the power line. It is also used as a bandpass filter, in order to reduce the harmonics of the transmit signal to a level of less than 52dBµV .

In receive mode, the line driver is switched off to avoid the low output impedance of the line driver attenuating the received signals and to save energy costs.

VI.2.1 - The Line Driver

The line driver has to amplify the output signal (ATO) of the ST7537 (see Figure 6).

First, a normal Push-Pull amplifier has been set up with two bipolar transistors Q4 (2N2222) and Q3 (2N2907). These types of transistors (2N2222 and 2N2907) have been chosen as they are cheap and widely used.

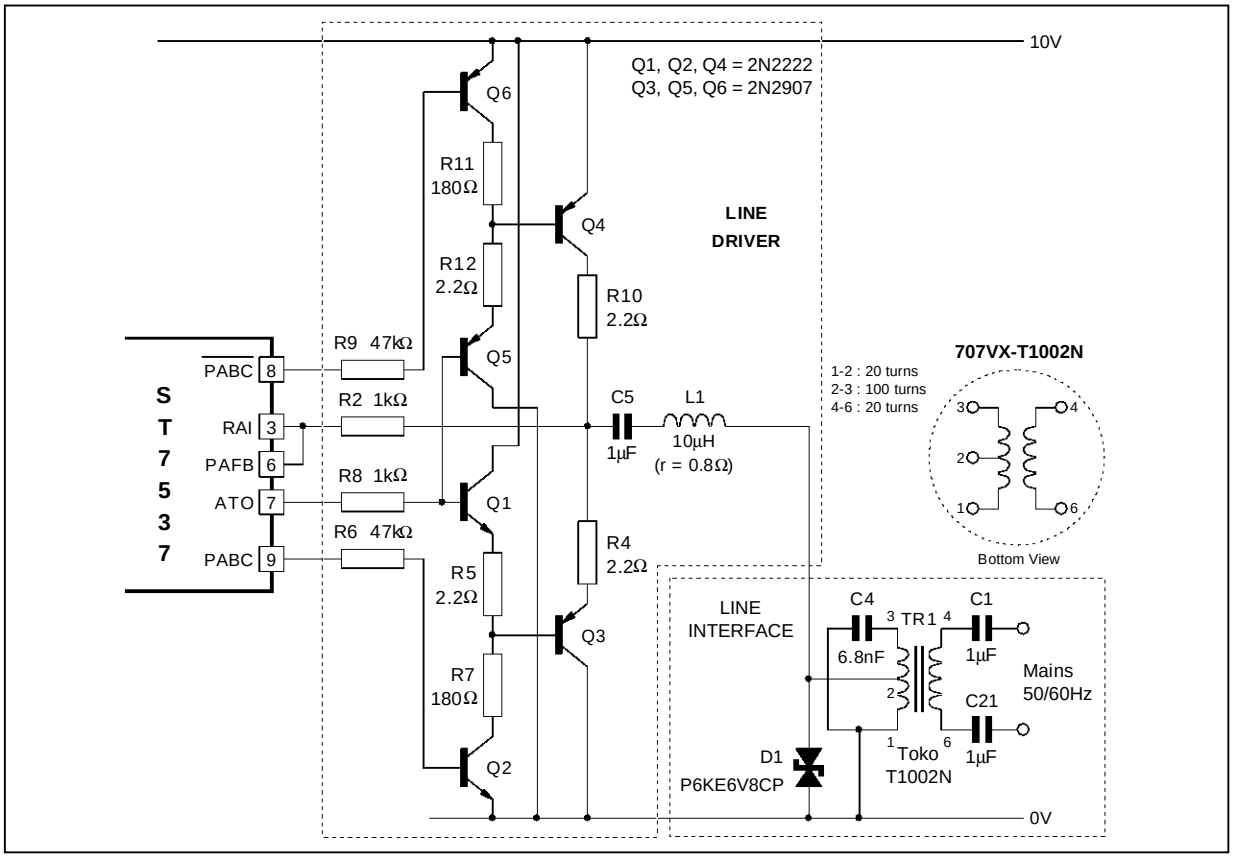
The resistors R4, R5, R10 and R12 degenerate the emitter of Q5, Q4, Q1, Q3 in order to define the bias current of the ouput branch independently of the mismatch of the transistors. The Push-Pull is polarized with two common collector amplifiers composed of Q1 (2N2222) and Q5 (2N2907). As far as resistors R7 and R11 are concerned, their value (180Ω) has been defined to obtain the optimum performances of the amplifiers thus define the bias current of the system.

The bipolar transistors Q2 (2N2222) and Q6 (2N2907) are used to switch off the power amplifier during the receive mode, thanks to the ST7537 output signals PABC and PABC which follow the Rx/Tx mode.

In order to avoid thermal runaways, it is mandatory to connect thermically Q1/Q4 and Q3/Q5. This is possible since the collectors of the transistors used are connected to the metal package. Consequently, both transistors will have the same temperature.

Main characteristics of the line driver :
- voltage gain = 1
- high input impedance
- low output impedance

Figure 6 : Power Line Interface Schematics



VI.2.2 - The Line Interface

In order to adapt the line driver to the power line, a transformer is used (see Figure 6). This transformer has :
- to isolate the rest of the interface from the power line
- to put the transmit signal on the power line
- to extract the received signal from the power line
- to filter 50Hz/60Hz signal coming from the power line
- to filter the harmonics of the transmit signal.

The used transformer is a TOKO T1002N. It has two primary windings and one secondary winding. The ratios of these windings are 4:1:1 (turns). Typical values of the transformer are :
- L1t windings : 9.4µH
- L4t windings : 140µH.

The primary windings of the transformer are used to create a bandpass filter. The resonance frequency is set at the transmit frequency with C4. This capacitor is in parallel with the primary winding (1t/4t). The equivalent value for those two windings can be calculated according to :

$$Leq = L1t + L4t + 2M$$

$$M = k \cdot \sqrt{L1t \cdot L4t}$$

With the given values :

$$k = 1/2^{1/2}$$
$$M = (9.4\mu H \cdot 140\mu H / 2)^{1/2} = 25.7\mu H$$
$$Leq = L1t + L4t + 2 \cdot M = 200.7\mu H$$

The resonance frequency of this LC network is dependant of C4 and Leq according to :

$$Fres = \frac{1}{2\pi \cdot \sqrt{Leq \cdot C4}}$$

$$C4 = \frac{1}{Leq \cdot (2\pi \cdot Fres)^2}$$

For Fres = 132.45kHz $\rightarrow$ C4 = 7.2nF (6.8nF is chosen since it is the nearest capacitor value available).

The capacitor C4 must be very linear in order avoid harmonic distortion. That's why a KS (styroflex or NPO ceramic capacitor) capacitor has been used.

In order to filter the 50Hz/60Hz signal from the powerlines, C1 is used. The capacitor filters the low frequencies (50Hz/60Hz) and lets the high (Transmit) frequencies pass. It is a class X2 capacitor. These capacitors have a short circuit protection, which is absolutely necessary. Indeed if a short circuit in the capacitor occurs, the 50Hz/60Hz filtering is lost, and the powerline interface will be destroyed, or worse, danger might occur for persons working with the interface and the ST7537. Moreover, since the TOKO transformer cannot overcome higher than 800V spikes, the safety norms are not met and the capacitor C1 is required to comply with them. An additional capacitor C21 is used as the phase location is unknown.

As a final protection against any possible spikes, a transil (TRL 1) is used. It is a 6.8V bidirectional type. If a voltage greater than 6.8V appears, voltage between pins of the system will be set to 6.8V, protecting the other parts of the power line interface from damage.

R1 is added to discharge C1 after disconnecting the interface from the powerline. Without this resistor, C1 will not be discharged and schock hazard might occur if someone touches the powerline connector. This resistor is only useful in evaluation systems. In all other cases where disconnection from the power line never takes place, R1 can be removed, saving undesired energy loss.

VI.2.3 - The Power Line Interface

The complete power line interface has been described in the two preceding parts. The interface has to be connected to the ST7537 as described in Figure 7.

The ATO and RAI are the analog output and input from/to the ST7537. The control of the transmit/receive mode is made with PABC and PABC signals from the ST7537. A high output (+10V) on PABC line selects the transmit mode, whereas a low output (0V) selects the receive mode.

The "pwr" outputs are the power line connections. On the application board, these connections are located close to C1 and the transformer in order to avoid long tracks carrying high voltage.

VI.2.4 - Performances of the power line interface

The following tests have been done on the power line interface :
- output impedance of the powerline interface versus the frequency
- Bit Error Rate (BER) test
- spectrum analysis of the transmit signal.

VI.2.4.1 - OUTPUT IMPEDANCE OF THE POWER LINE INTERFACE VERSUS THE FREQUENCY

The output impedance of the power line interface is measured with an impedance analyzer as it is shown in Figure 8. The board is set in receive mode.

The results are given in annexe B.

Test equipment : 41924 LF Impedance Analyzer 5Hz-13MHz (Hewlett Packard)

Test conditions : T = +25°C

Figure 7 : Power Line Interface Inputs and Outputs

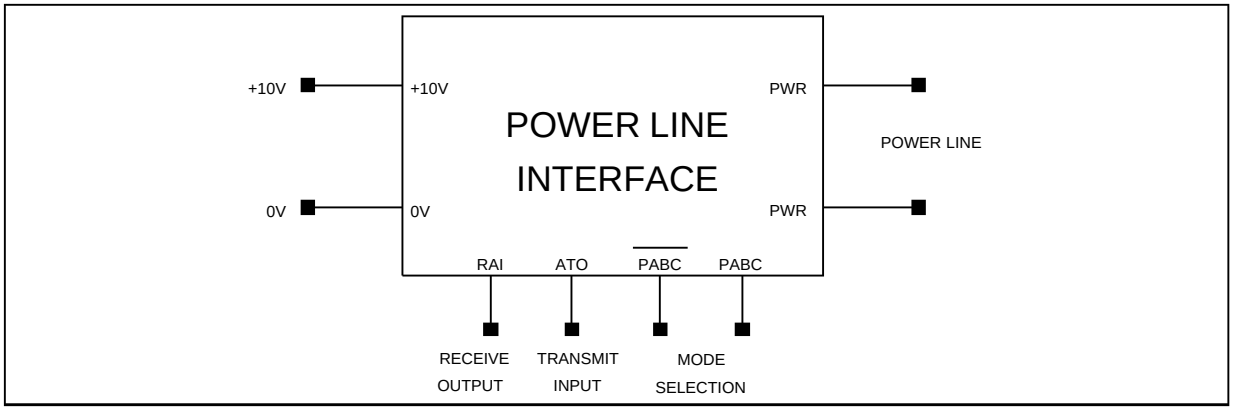
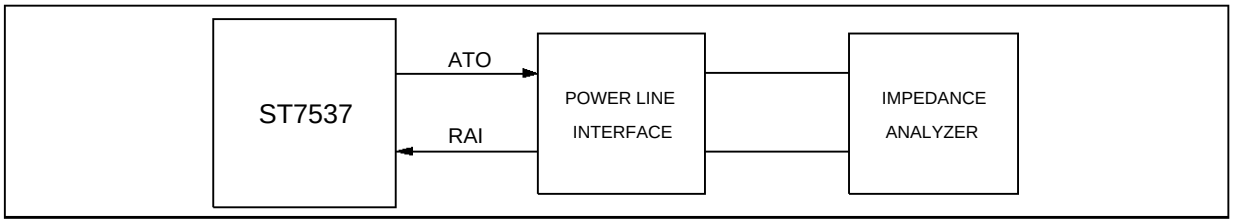


Figure 8 : Output Impedance Measurement Configuration



VI.2.4.2 - BER TEST

Two boards are required : one for the transmission, the other one for the reception.

White noise is added to the ATO transmit output of the ST7537 thanks to a mixer. The aim is to measure the BER under different Signal/Noise ratio conditions. The mixed signal is transmitted to the RAI receive input of the modem. The digital signal injected in TxD is a 2^{15}-1 pseudo-random pattern long, generated by a bit error rate analyzer (with internal 1.2kHz asynchronous clock).

In the reception board, a 1.2kHz clock (CRX) is built thanks to the ST7537 MCLK clock. The received digital signal RxD is amplified (RxDL) and synchronized with the CRX clock. Both of them (CRX and RxDL) are analyzed by the BER analyzer.

The measurements are made with different RAI input level. The Figures 10 and 11 gives respectively the B.E.R with a RAI input level of 10.023mV$_{RMS}$ and 1.14mV$_{RMS}$.

Conclusion

Under the test conditions of the ST7537 specification (RAI = 10mV$_{RMS}$ and S/N = 15dB) the BER is 4.10-7. With an RAI input level of 1.14mV$_{RMS}$ the BER is around 10-4 with the same S/N ratio. Therefore, the ST7537 is able to communicate with low input signal level of about 1mV$_{RMS}$. This test illustrates the high sensitivity of the power line modem.

In Figure 10, the measured BER (with an RAI input level of 10mV$_{RMS}$) is compared with the theorical BER of a conventional BFSK modulator/demodulator.

Test equipment : SI7703B BER analyzer
Rhode and Schwartz noise generator

Test condition : T = +25°C

Figure 9 : BER Test Configuration

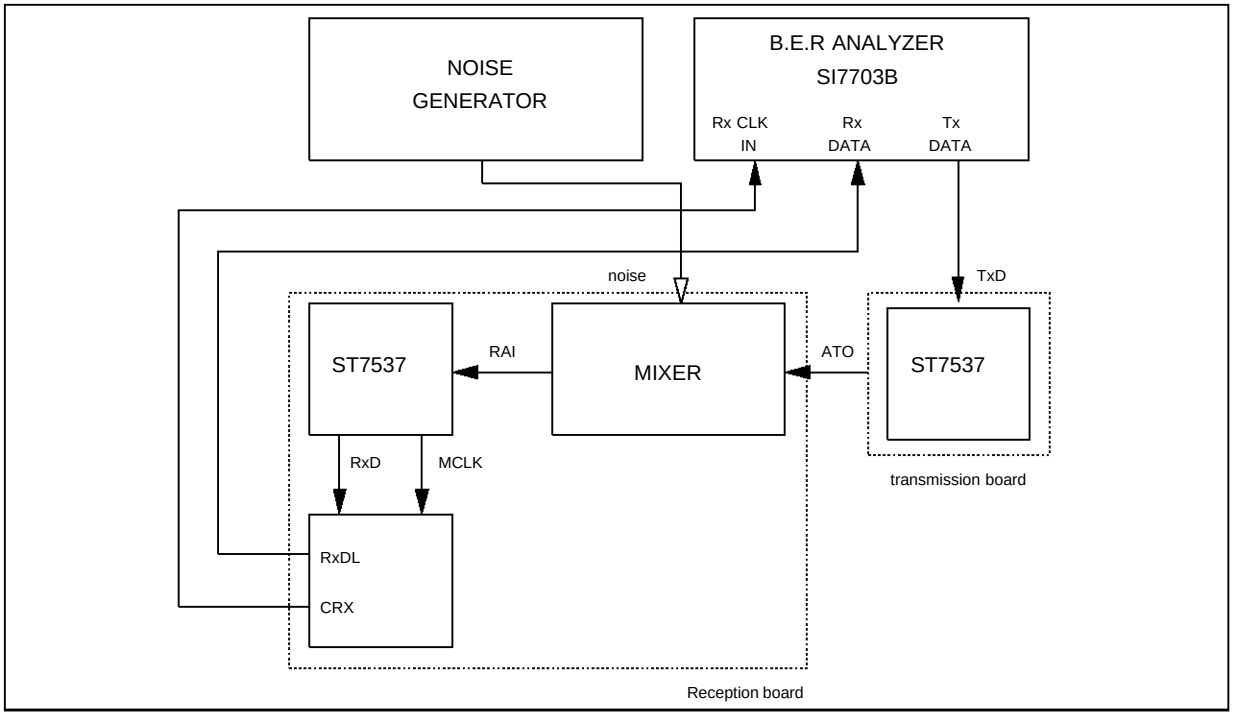


Figure 10 : BER Test for an RAI Input Amplitude of 10.023mV$_{RMS}$

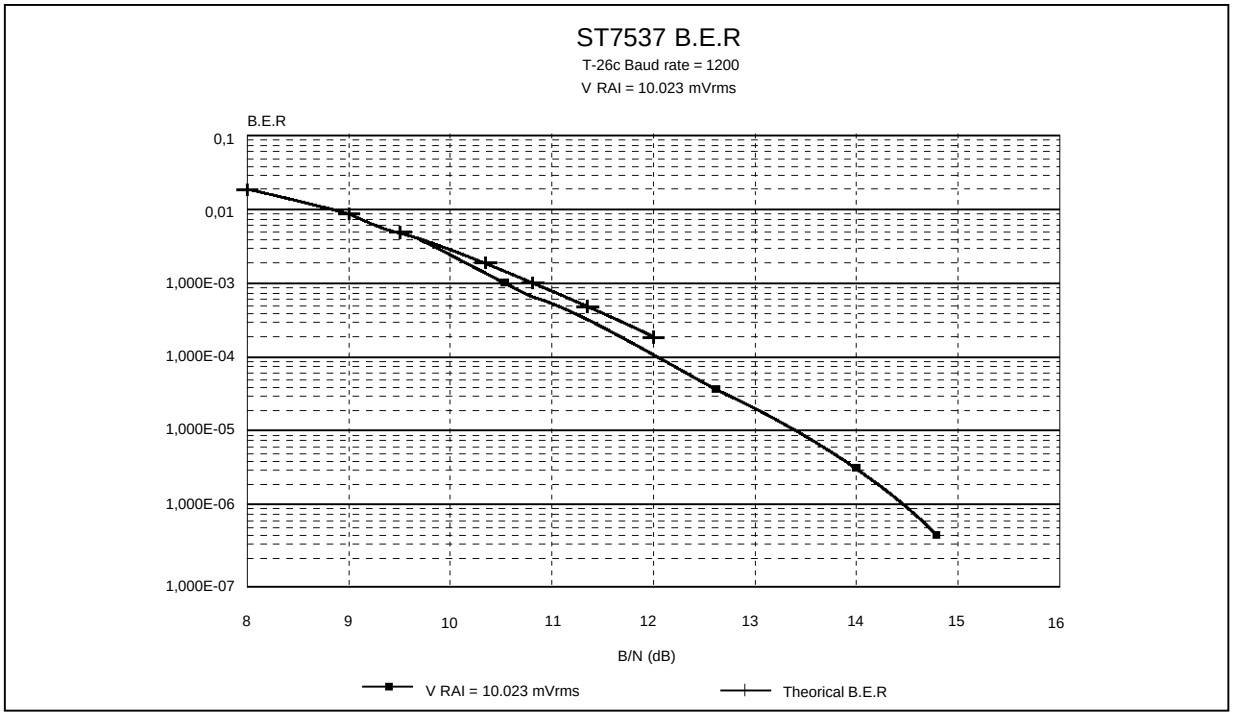
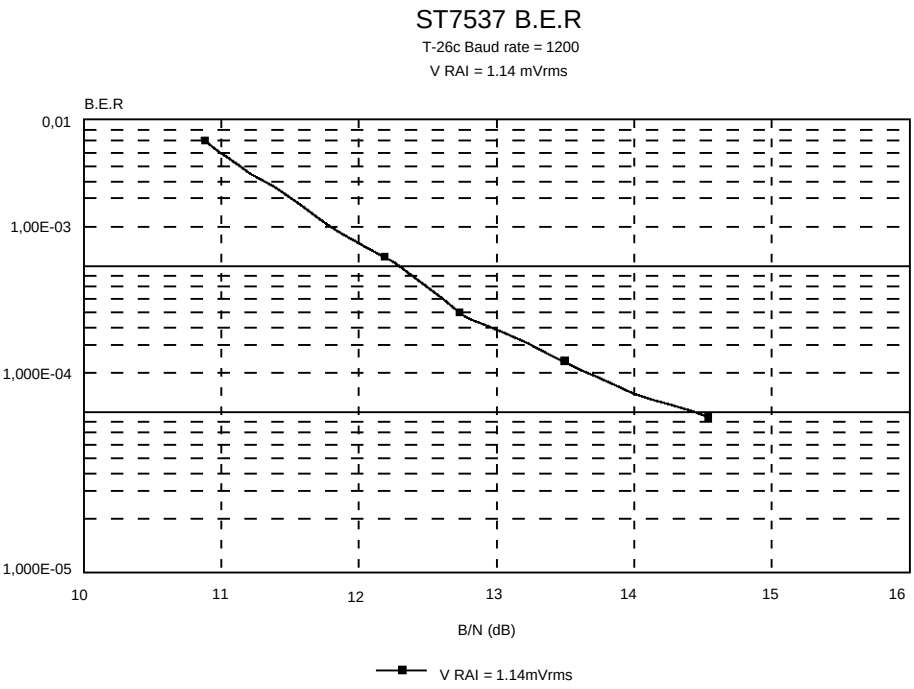


Figure 11 : BER Test for an RAI Input Level of 1.14mV$_{RMS}$



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VI.2.4.3 - TRANSMIT SIGNAL SPECTRUM ANALYSIS

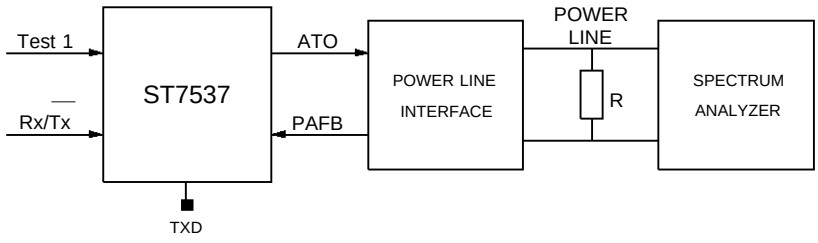
The transmit output signal of the power line interface is measured with the power line simulated by resistors : R = 1, 5, 10, 50, 100Ω.
A spectrum analyzer is used to display the output signal frequency spectrum of the power line interface (see Figure 12).

In a first design of the board, a 2.2Ω resistor was used instead of the inductance L1. In this configuration, whatever the power line impedance, the output level was at least 106dBµV up to 119dBµV (see Figure 13). Thus no communication problems had been noticed during the test session.
To improve the frequency spectrum of the transmit signal, the resistor has been replaced by an inductance L1 of 68µH, 1.6Ω (see Figures 14 and 15).

However, tests on a real site showed that the transmit level was very low with this inductance in case of low power line impedance : with an impedance of 1Ω, the output level is 87dBµV, so that communication difficulties occur. At the transmit frequency (132.45kHz), the inductance looks like an impedance of about 56Ω, which introduces significant attenuations on the transmit signal compared to those induced by the 2.2Ω resistor.

To improve the output signal amplitude, the inductance value must be modified. A compromise has to be found between filtering the pertubation voltages and lowering the impedance of the inductance at the transmit frequency. An inductance of 10 µH (0.8Ω) has been chosen which looks like an impedance of 8Ω at 132.45kHz frequency (see Figures 16 and 17).

Figure 12 : Spectrum Analysis Configuration



R : 1/5/10/50/100 ohm
TXD : "0" / "1" (0V / +5V)

7537-18.AI

Figure 13 : Output Transmit Level (dBµV) with 2.2Ω Resistor

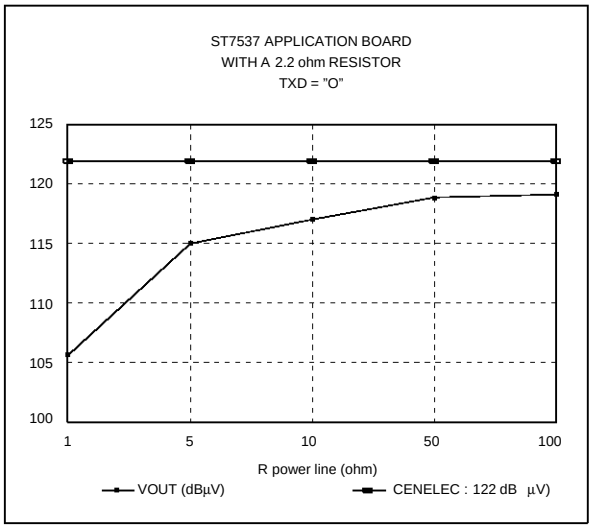


Figure 14 : Output Transmit Level (dBµV) with 68µH Inductance

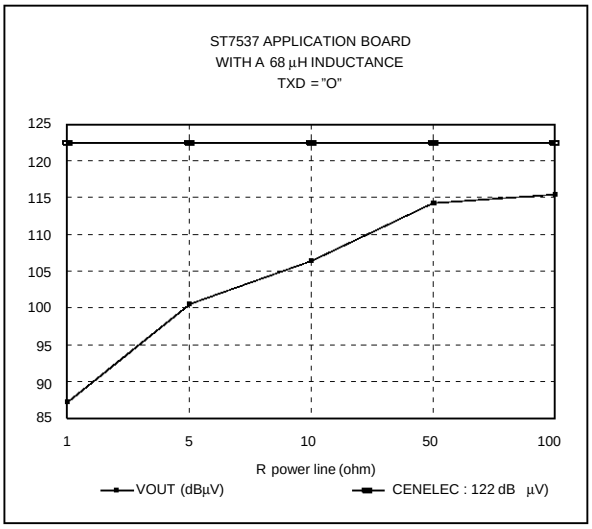


Figure 15 : Second and Third Harmonics Level (dBµV) with 68µH Inductance

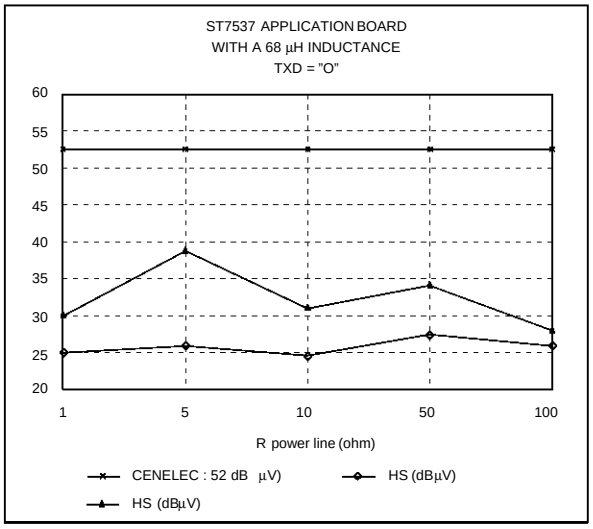


Figure 16 : Output Transmit Level (dBµV) with 10µH Inductance

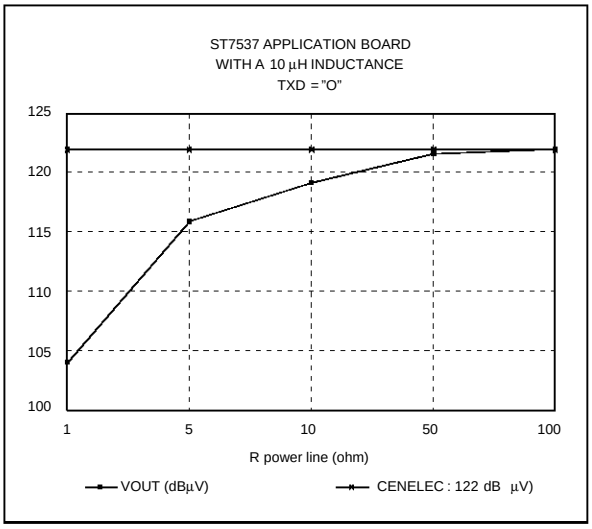
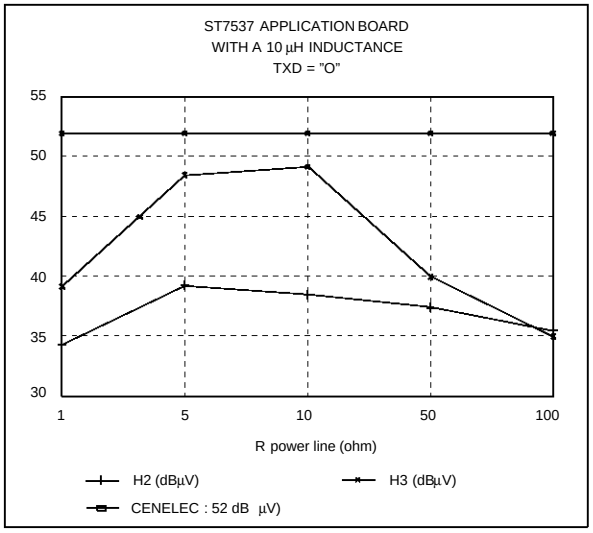
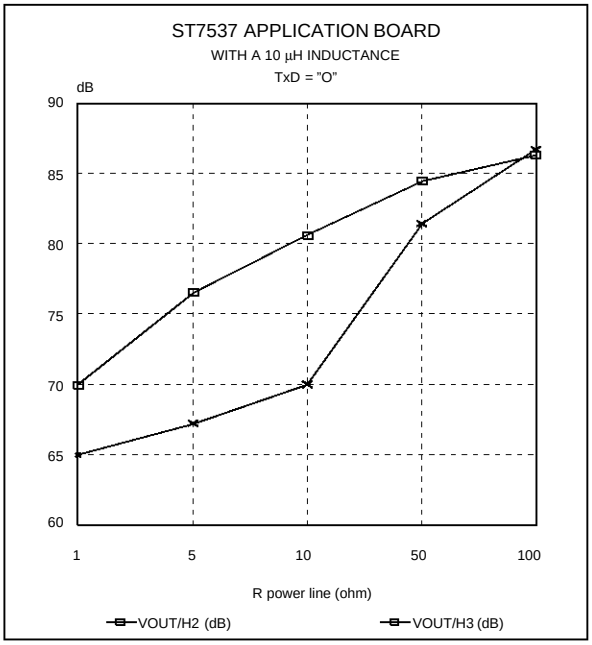


Figure 17 : Second and Third Harmonics Level



VOUT/H2 and VOUT/H3 variations with the 10µH inductance versus the power line impedance are given in Figure 18.

Figure 18 : Demoboard Transmit Performances



Test results (with L1 = 10µH)	CENELEC specifications	FCC specifications
VOUT < 122 dBµV	VOUT < 122 dBµV,	
H2 < 39 dBµV	H2 < 56 dBµV mean	H2 < 48 dBµV (extended to 60 dBµV)
H3 < 49 dBµV	H3 < 52 dBµV mean	H3 < 48 dBµV (extended to 60 dBµV)
VOUT/H2 > 70 dB		
VOUT/H3 > 65 dB		

Conclusion

With L1 = 10 µH, the required harmonics level is reached and the output voltage is smaller than 122 dBµV. Therefore, the power line interface is fully operating according to the CENELEC and FCC specifications. Moreover, for very low power line impedances, the output transmit level is high enough to ensure a good communication quality.

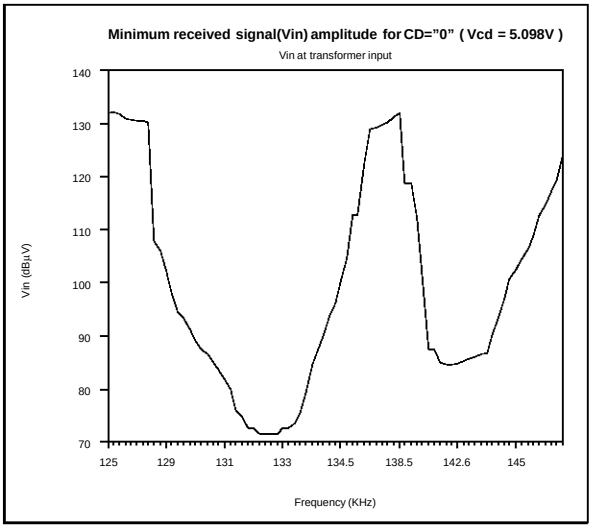
Test equipment : 3585A Spectrum Analyzer 20Hz-40MHz (Hewlett Packard)
Test conditions : T = +25°C

VI.3 - Carrier Detect

The carrier detect output ($\overline{CD}$) is driven low when the input signal amplitude on RAI is greater than V_{CD} typically $5mV_{RMS}$ for at least T_{CD} (typically 4ms). When the input signal disappears or becomes lower than V_{CD}, $\overline{CD}$ is held low for at least T_{CD} before returning to a high level. V_{CD} input is the carrier detection threshold voltage which is set internally.

The graph, given in Figure 19, represents the minimum amplitude of the received signal which can be detected (which corresponds to $\overline{CD}$ = 0) according to the frequency. Thus input signals at a frequency of 133.05kHz (high logic level) and 131.85kHz (low logic level) can de detected at a very low level. For frequencies smaller than 129kHz or greater than 150kHz, the detection is made at a very high level of input signal. Therefore, only significant frequencies received signals are detected.

Figure 19 : RAI Input Minimum Detection Level



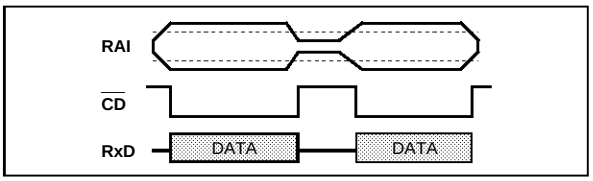
7537-61.AI

VI.4 - Improving Sensitivity

In all modem, the carrier detector clamps the outgoing digital data RxD when the incoming analog receive signal is below a defined level (carrier detector level 7537 typ = $5mV_{RMS}$).

That means we are loosing the data when the signal is less than $\overline{CD}$ level.

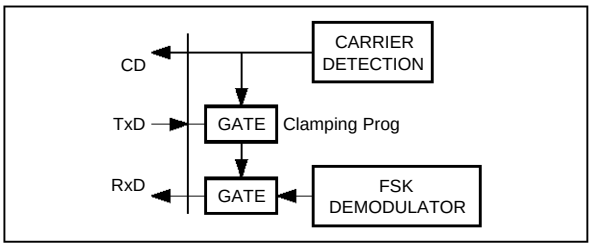
Figure 20



7537-40.EPS

In the ST7537, the clamping of $\overline{CD}$ on RxD is programmable thanks to TxD pin.

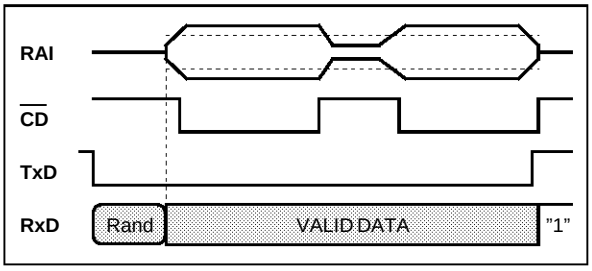
Figure 21



7537-41.EPS

So we are able to receive data even if the incoming analog receive signal is less than 5mV. When removing the clamping of RxD by $\overline{CD}$ we are able to get RxD data without error with a receive level of 400 micro Volt.

Figure 22



7537-42.EPS

As you can see on previous Figure even when RAI is lower than the carrier detect level we get the datas because TxD = "0".
When TxD = "0" and the receive signal is not one of the 7537 (e.g Noise), the RxD is random (in most configuration the RxD is at "0").

Example of Implementation

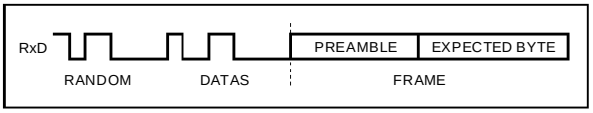
We have seen that by programming the TxD to "0" in receive mode we increase the sensitivity of the ST7537 because there is no more clamping by $\overline{CD}$. You will be able to have good communication with a receive signal of around 50dBµV which means a dynamic of around 70dB.

Because we want to get the benefit of the very good sensitivity of the ST7537, we will program TxD to "0" in receive mode and create by soft a frame detector. We will use the CD signal as mentionned by CENELEC only when we want to transmit a frame.

Different software frame detector can be implemented depending of the ressources of your microcontroller.

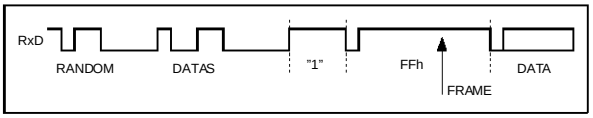
You can program your microcontroller to go in receive frame when it received the expected byte.

Figure 23



So the preamble is for demodulator training (when you start a communication the 3 first bits are lost by the receiver) and when you will match with expected byte the microcontroller will go in receive frame routine.
On the ST6 microcontroller we have implemented the following frame detector.

Figure 24



We put TxD = "1" on the transmitter for around 4ms (for demodulator training) and after we send in asynchronous mode FFh following by the complete frame.
On the receiver, we check that we have RxD equal to "1" for at least 7ms (we are looking for FFh), then we go in receive and we will have frame synchronization on the first start bit of the data.
We did a trial in our lab with this system during 2 hours without having the ST6 going in frame receive routine on bad datas dued to noise signal.

VI.5 - Communication with a RS232C Interface

The application board can be connected to a Personal Computer (PC) thanks to the RS232C interface. As the electrical levels of the RS232 port (±12V) do not match the electrical levels of the ST7537 (TTL levels 0/+5V), a MAX232 is used to make communication possible. This device has two RS232 receivers to convert RS232 levels into TTL levels and two RS232 transmitters to convert TTL levels into RS232 levels. The connections between the ST7537 and the RS232 interface are given in Figure 25. Not all the pins from the RS232 port are used. The RXD, TXD and Carrier Detect (CD) signals are directly converted. The Request To Send (RTS) line is used to set the ST7537 in receive or transmit mode, but also to give the PC a Clear To Send (CTS) signal. The Data Set Ready (DSR) line is connected to the Data Terminal Ready (DTR) line. This simulates the transmission of the DSR signal by the power line modem when the PC is ready. The RI output of the PC is only used for telephone network modems, and therefore it is not connected. If the RS232 port of the PC is used, it is necessary to provide the board with a watchdog clock (e.g : 1kHz) in order to get the PC communication working. A suggested clock generator is given Figure 26. It uses a NE555 timer working in astable mode.

The output HIGH time of the clock is :
$t_H = 0.693*(R1 + R2)*C1$

The output LOW time of the clock is :
$t_L = 0.693*(R2)*C1$

Thus the total period T is : $T = t_H + tL$
The frequency of oscillation is : $f = 1/T = 1/(t_H + t_L)$

Calculations provides the following results :
R1 = 1kΩ, R2 = 100kΩ, C1 = 7nF.

Figure 25 : Connections between ST7537 and RS232 Interface

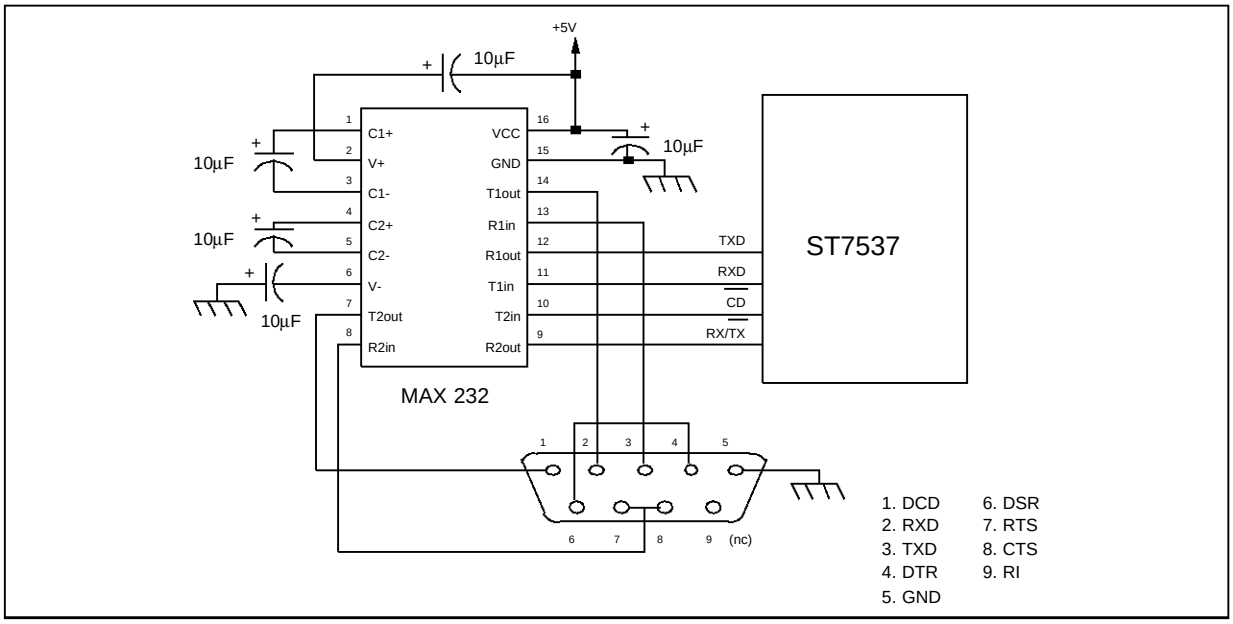
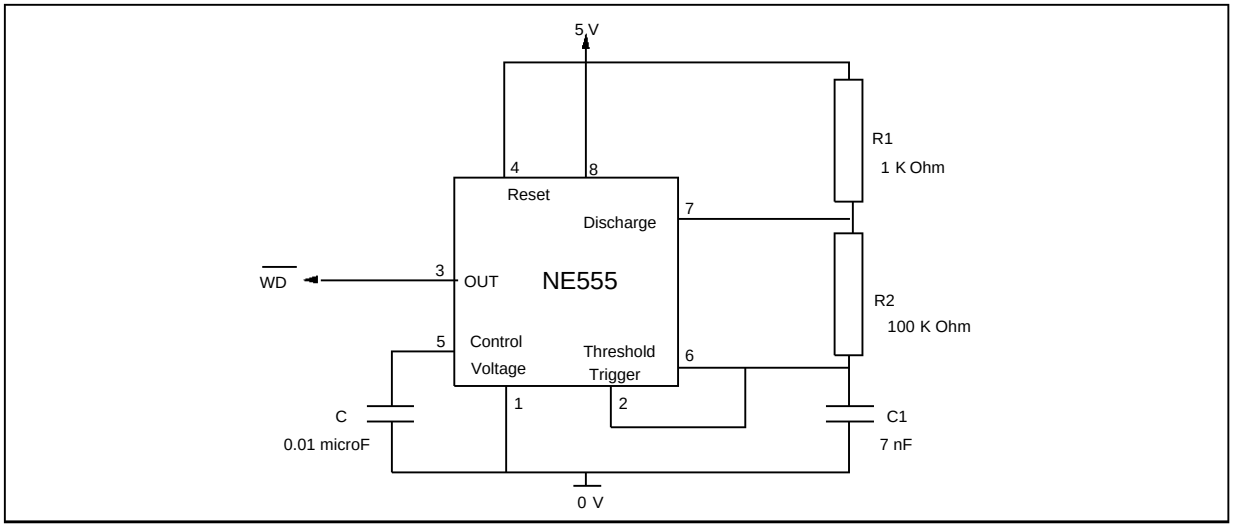


Figure 26 : Watchdog Clock



RS232C Communication Problem

We have discovered that with some computer the communication program does not work correctly. In some new PC generation the UART is sensitive to the RxD jitter and then shows characters errors on PLM communication.

The following hardware avoid the jitter on RxD for the UART of the PC.

Figure 27

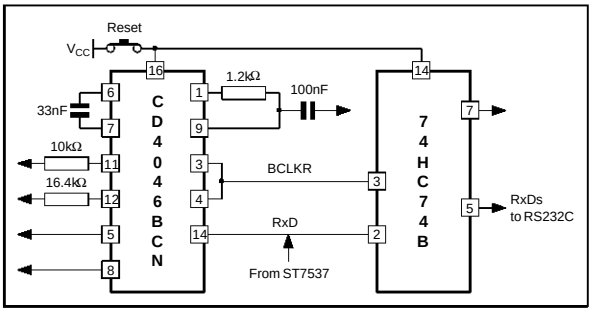
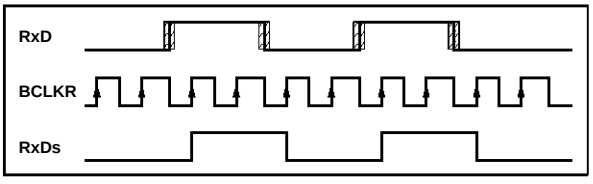


Figure 28



After power-up the 7537 demoboard, you have to reset the receive recovery block.

Before doing this extra hardware we recommend you to test your PC with the new program and if there are time to time some errors the hardware has to be adapted as shown above (you can use BCLKR for the watchdog clock).

VI.6 - Demoboard Communicating Application

The ST7537 power line modem enables you to design ”communicating” appliances, which meet your specific requirements and comply with the CENELEC specifications. Equipped with a single low-cost ST90E28 microcontroller, it makes it possible to build a ”smart” home network, where each device is able to use any information required either if it is local (sensors) or remote (inside any other communicating appliance).

This paragraph is intended to provide design basics for the implementation of the ST90E28 on the ST7537 demoboard.

VI.7 - Overview of the ST90E28 MCU

The ST90E28 microcontroller chosen to equip the ST7537 demoboard is a 16Kbyte program memory EPROM version with 256 bytes of RAM and 256 bytes of register file. Within this file, 224 general purpose registers are available as RAM, accumulators or index pointers, allowing code efficiency. This MCU has an internal clock generator, a 16-bit watchdog timer for system integrity, a powerful serial communications interface (SCI) with included baud rate generator and outstanding character search capability, and a 16-bit multifunction timer for complex user applications; it provides a reset input and up to 36 input/output pins, including 7 external interrupts and a non-maskable interrupt.

Most of the instructions take 14 clock cycles: with a clock frequency of 11.0592MHz, one instruction lasts about 90ns. Connected to the ST7537, the microcontroller has to deliver a maximum bit rate of 1200 bauds: one bit is at least 833µs long.

VI.8 - Implementation of the ST90E28 MCU

Two configurations have been set up, one for the slave appliances, and one for the master system. Both versions will have their address initialized in the software in this first release. Besides, they use one data output to display information about the main program execution by means of a led: you know that the main program is running well, when this led is blinking as the appliance is powered on. The main differences between the two controllers are the input/ouput facilities.

The slave configuration provides an ouput that switches a load. This load will be simulated by a LED (see Figure 29).

The master configuration provides a 3-bit command input to control the slaves. This command will be simulated by a KEYBOARD : one key is available for each slave, and one specific key enables the user to supervise all the slaves inside a room at once. This configuration also uses a 3-bit data output to let you know whether a particular slave is on, or whether the room is lit up. This information will be displayed by one led attached to the key dedicated to a particular device (see Figure 30). All the slaves addresses will be stored in the master version of the software.

Furthermore, both configurations need a 7 bit data exchange with the ST7537 : clock, transmit data, receive data, reset, Rx/Tx control lines (see Figure 31). No external component is needed to interface the microcontroller with the power line modem, allowing cost savings.

- OSCIN (Pin 2) : The MCU oscillator is driven with the PLM master clock, so that no additional crystal is needed. In this case, the oscillator output pin must stay unconnected.
- Port 5 bit 1 (Pin 42) : This output bit provides the PLM watchdog input with negative transitions, before the timeout end is reached. The watchdog pulses must be at least 500ns wide with a period of at least 800µs and up to 1.5s.
- Port 5 bit 0 (Pin 43) : This output controls the Rx/Tx mode. When this bit is 0, the transmit mode is set, otherwise the receive mode is selected. Remember that the ST7537 switches automatically in the receive mode, when this bit is held at 0 longer than 1s.
- INT1 (Pin 26) : The PLM carrier detect signal channels through this external interrupt input pin, which is triggered on falling edge. On signal detection, the carrier detect output is driven low and generates an interrupt request.
- SOUT (Pin 30) : The microcontroller provides the ST7537 with Tx data by means of the SCI output.
- SIN (Pin 31) : The ST7537 provides the microcontroller with Rx data through the SCI input.
- NMI (Pin 18) : The PLM reset output signal acts as an MCU external watchdog, in order to detect hardware or software failures. This signal channels through the MCU external non maskable interrupt input pin, which is triggered on rising edge. When the power supply is too low or when no negative transition occurs on the PLM watchdog input for more than 1.5s, the reset ouput is driven high and generates a top level interrupt request, which resets the microcontroller. As for the MCU internal watchdog timer, the watchdog mode is disabled, so that a second 16-bit programmable timer is available for customer applications.

Figure 29 : Slave Configuration

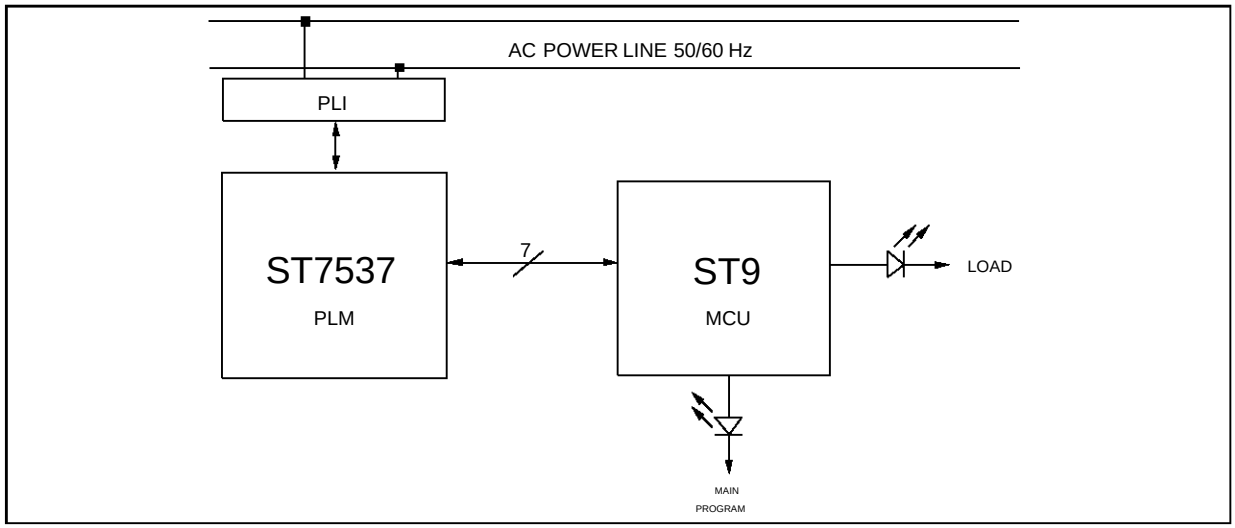


Figure 30 : Master Configuration

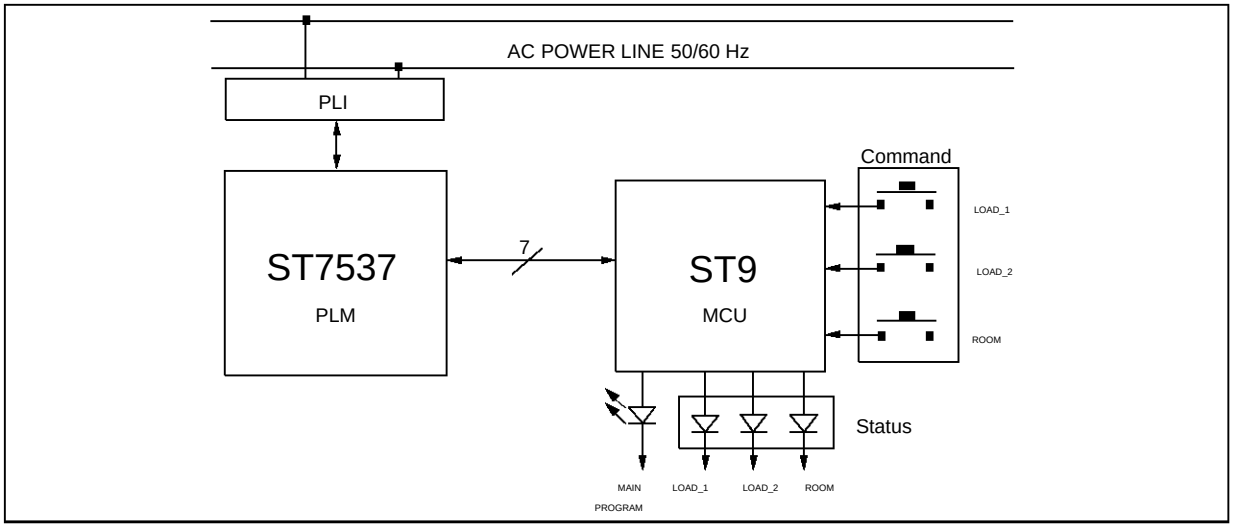
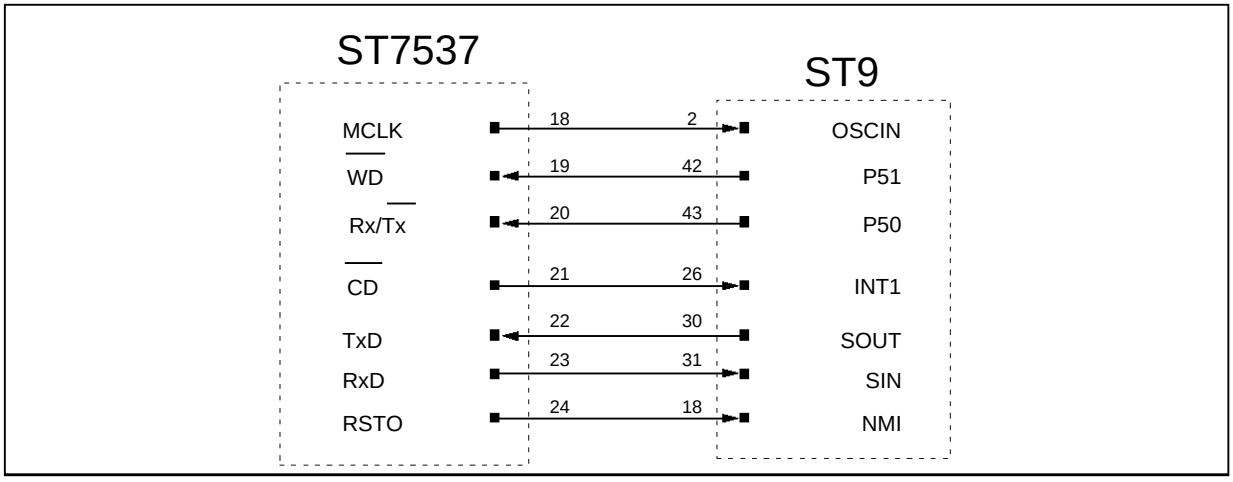


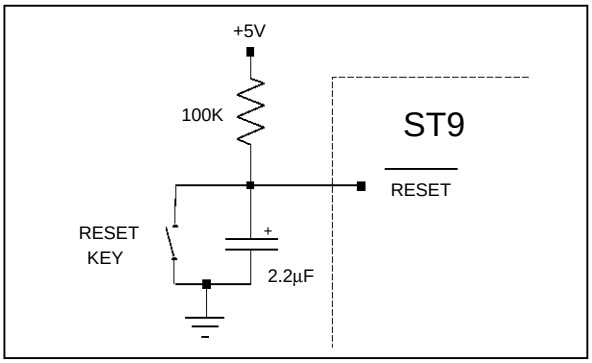
Figure 31 : Interface between ST7537 and ST90E28



VI.8.1 - Applicative Pin Configuration

- V_{SS} (Pin 1) : Digital Circuit Ground
- V_{DD} (Pin 21) : Main Power Supply Voltage +5V. A decoupling capacitor of 47µF is connected between V_{DD} and V_{SS} pins. The V_{DD} of the microcontroller should be connected also to the DV_{CC} of the ST7537 in order to reference the digital level of the ST7537.
- RESET (Pin 3) : This input is active low. To restart the microcontroller, the reset key has to be pressed (see Figure 32). A capacitor (2.2µF) will keep the input low for a minimum startup period, whereas a pull-up resistor (100kΩ) will keep it high for normal operation.

Figure 32 : Reset Command



- Display Output : Light emitting diodes are used to display data. The maximum current provided by each output pin is 0.8mA. Therefore the serial resistor R has a minimum value of 4.7kΩ (see Figure 33 : current = (4.2-0.6)/4.7e3 = 0.77mA).

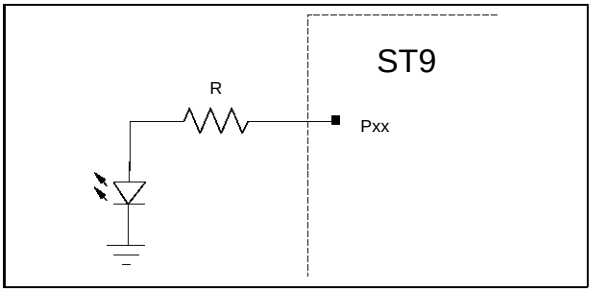
  The slave configuration uses 2 display output pins.

  Port 2 bit 3 (Pin 25) : blinking led
  Port 2 bit 5 (Pin 27) : load (slave led)

  The master configuration uses 4 display output pins.

  Port 2 bit 3 (Pin 25) : blinking led
  Port 2 bit 5 (Pin 27) : load 1 status
  Port 2 bit 6 (Pin 28) : load 2 status
  Port 5 bit 5 (Pin 38) : room status

Figure 33 : Display Output

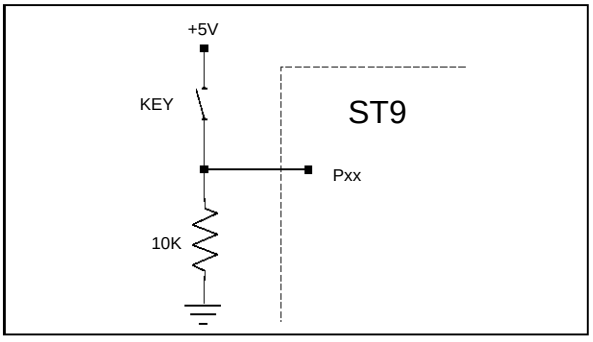


- Keyboard Input : Switch keys are used to enter commands. The keyboard pin is active high (see Figure 34). A pull-down resistor of 10kΩ keeps the input low, whereas a key press holds it high for active operation.

  The master configuration uses 3 keyboard input pins.

  Port 5 bit 2 (Pin 41) : load 1 command
  Port 5 bit 3 (Pin 40) : load 2 command
  Port 5 bit 4 (Pin 39) : room command

Figure 34 : Keyboard Input



VI.8.2 - Power Consumption

The power consumption of each configuration has been measured. Both master and slave boards were connected to the AC power mains : the slave led and all master status leds are switched ON by pressing the master room key (worst case simulation).

The current consumption is measured with a digitizing oscilloscope (channel 2) by means of a serial resistor, which value is small enough to avoid big supply voltage drops (about 1Ω typically).

A dual tracking power supply provides each board with the same power voltage, which value is displayed on a multimeter.

Test equipment : Fluke 45 Multimeter, Tektronix TDS460 Digitizing Oscilloscope
Test conditions : R = 1.04Ω , Valim = +10.006 V
T = +25°C

- Slave board : the oscilloscope is triggered on the falling edge of the Carrier Detect (CD) signal displayed on channel 1 (see Figure 35). Therefore, the current consumption is displayed on channel 2 in receive mode on stand-by (CD = 1) and active (CD = 0) states.
  Current consumption (Rx mode) :+146mA$_{RMS}$
  Power consumption :
  (+10.006V - 1.04Ω · 146mA) · 146mA = +1.44W

  Slave board current consumption test results (see Figure 36)
  Channel 1 : Carrier Detect signal
  Channel 2 : Supply current

- Master board : the oscilloscope is triggered on the falling edge of the Rx/Tx signal on channel 1 (see Figure 37). The current consumption is displayed on channel 2 in both receive and transmit modes.

  Current consumption :
  Rx mode +160mA$_{RMS}$
  Tx mode +230mA$_{RMS}$

  Power consumption :
  Rx mode (+10.006V - 1.04Ω · 160mA) · 160mA = +1.57W
  Tx mode (+10.006V - 1.04Ω · 230mA) · 230mA = +2.25W

Master board current consumption test results (see Figure 38)
Channel 1 : Rx/$\overline{Tx}$ signal
Channel 2 : Supply current

Figure 35 : Slave Board Current Consumption Test

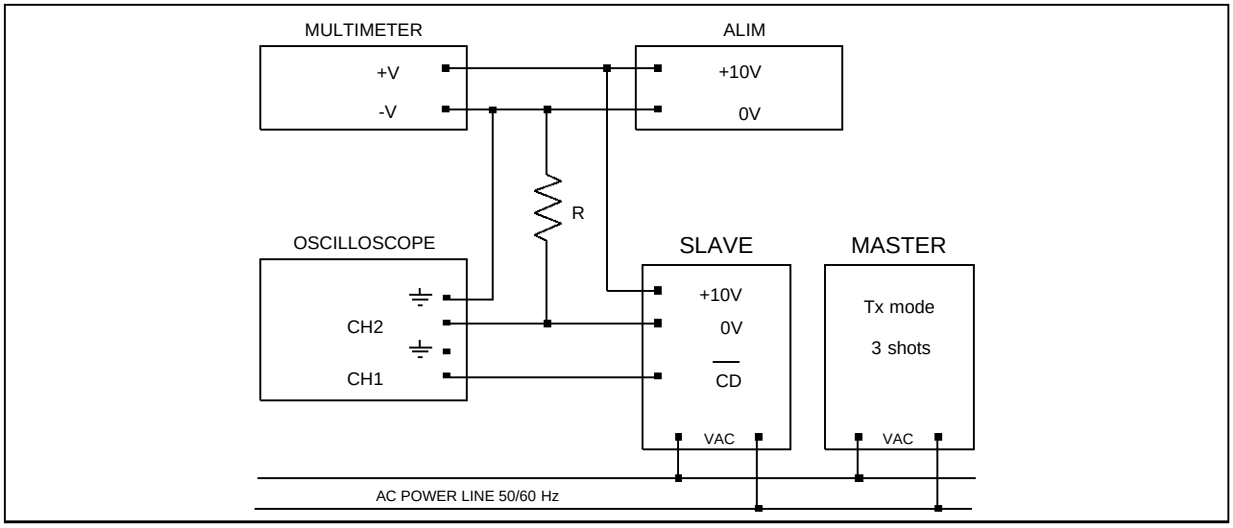


Figure 36 : Slave Board Current Consumption Test Results

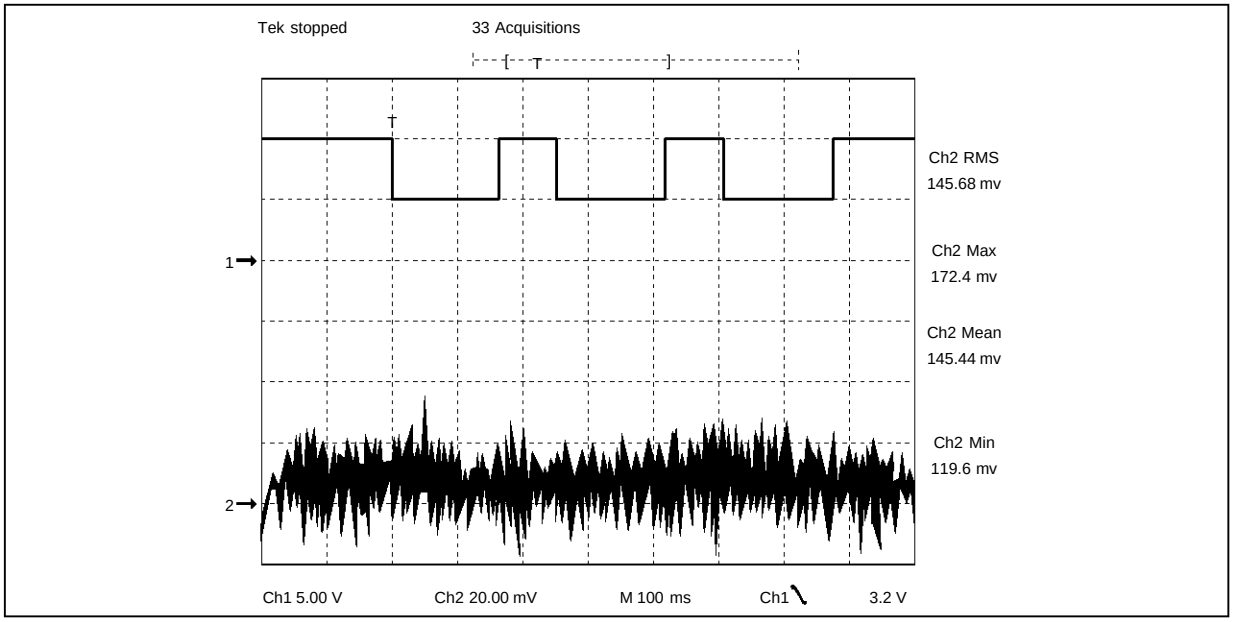


Figure 37 : Master Board Current Consumption Test

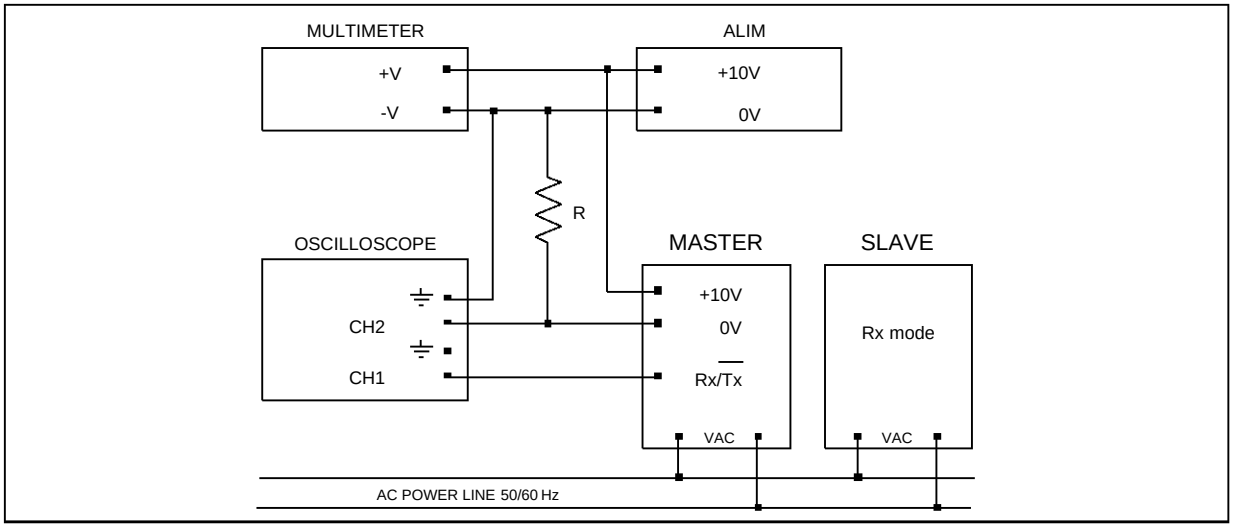
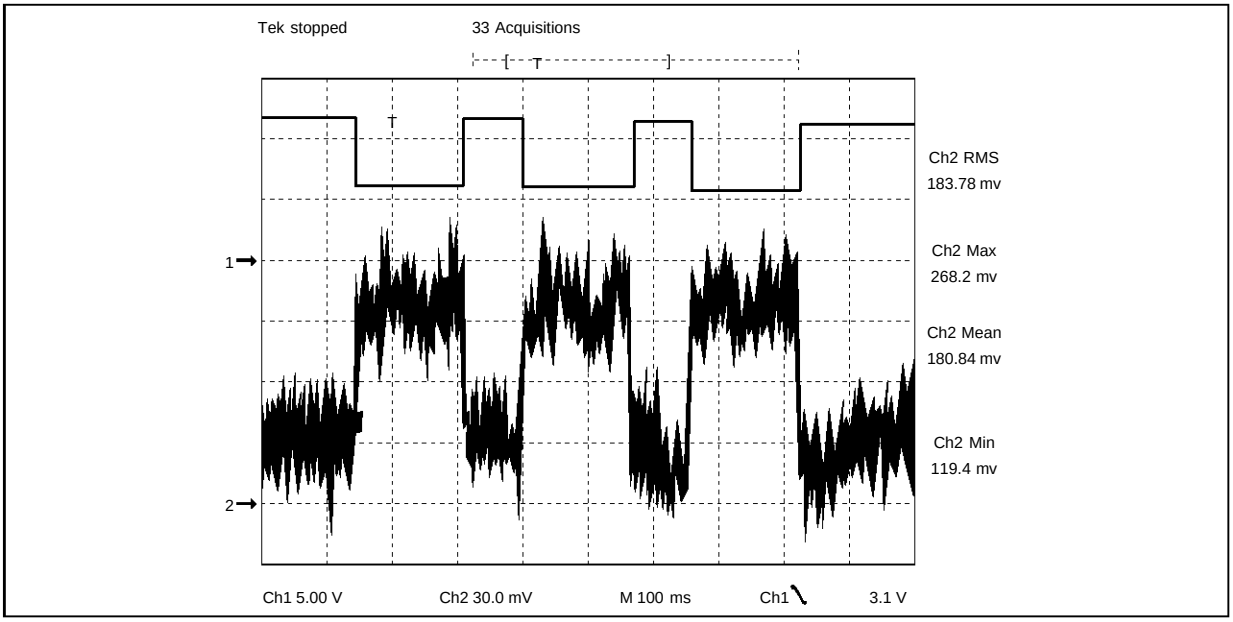


Figure 38 : Master Board Current Consumption Test Results



V.9 - Power Supply

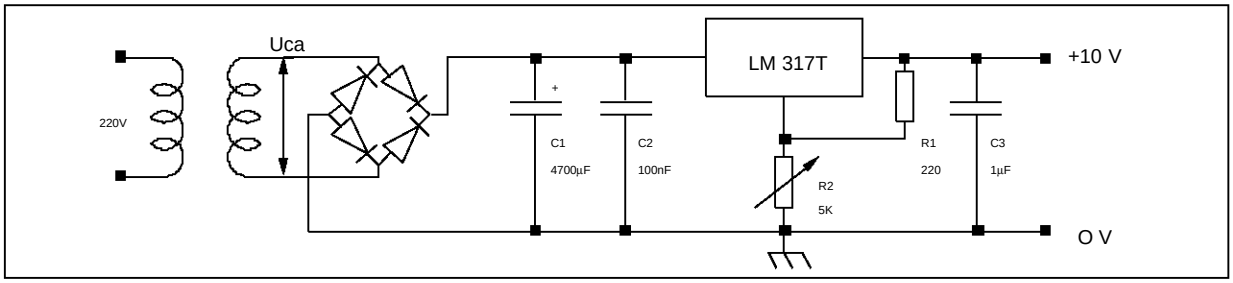
V.9.1 - Power supply features

The power supply features are :
- one reference voltage of 10 V_{DC}
- output current of 400 mA

The 5 V_{DC} voltage needed for the numeric part of the application is provided by a voltage regulator LM 7805, which already exists on the board.

The power supply schematic is given in Figure 39 : The LM317T regulator is ajustable between 1.2V and 37V thanks to the R1 & R2 resistors. It could be replaced by a +10V regulator.

Figure 39 : Power Supply Schematics



V.9.2 - Power supply sizing

The rectified voltage between pins of the capacitor C1 is shown in Figure 40 :

Uca = transformer secondary voltage (V_{RMS})
Ucc = voltage between pins of the capacitor C1
Urtt = ripple voltage
U = minimum voltage which has to exist between input and output of the voltage regulator
Us = output power supply voltage
Ud = rectifier diodes voltage drop
I = output power supply current

Hypothesis :
- I = 400mA
- Umin = 3V
- Ud = 1V

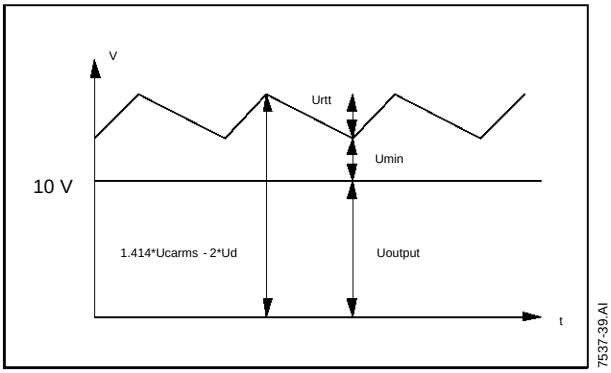
The minimum voltage the transformer has to provide is :

$$Uca = (Us + Umin + Urtt + 2Ud) / 2$$

The ripple voltage is :

$$Urtt = 10 * I / C1 \text{ (with I in mA and C1 in } \mu F)$$

Figure 40 : Rectified Voltage Parameters



V.9.3 - Using a 2x6 V secondary voltage transformer

The transformer must be able to supply I = 400mA, so that a 5 VA transformer is required.

The maximum value of Urtt is :

$$Urtt\ max = 2*Uca - Us - Umin - 2*Ud = 2V$$

$\Rightarrow$ C1 min = 10*I / Urtt max
C1 min = 2000µF

We choose a C1 capacitor value of : 4700µF

The maximum voltage Vmax which can be applied between C1 pins has to be higher than the maximum secondary voltage of the transformer. Therefore, with a safety margin of 25% :

$$Vmax = (2 * Uca) * 1.25 = 21.2V$$

The maximum power dissipated by the voltage regulator is :

$$Pd = U * I$$

U = 2*Uca - Us - Urtt - 2*Ud
Urtt = (10 * 400) / 4700 = 0.85V
$\Rightarrow$Pd = 1.6W

In short, the power supply sizing is :
- secondary voltage of the transformer : 2x6V
- 5 VA transformer
- C1 = 4700µF with a maximum voltage of 25V between its pins.

VII - PC SOFTWARE

With the application board, we provide you a communication program written in Turbo C language which allows :
- to drive the RS232 interface
- to transmit data via power lines thanks to the ST7537
- to receive data from power lines thanks to the ST7537
- to process data
- to run character error test.

It is possible to transmit :
- characters
- text (maximum 80 characters)
- hexadecimal data (maximum 64 bytes)
- file.

The communication program allows you to run different types of communication :
- communication between 2 computers.
- communication between 2 ports COM on the same computer.

VIII - TYPICAL APPLICATION

VIII.1 - Protocol Design

The software described in the following parts provides you with a simple efficient protocol kernel, which is fully interrupt handled and uses almost no CPU time. Therefore it enables you to develop friendly interactive applications with a short response time.

This protocol uses a packet encapsulation mechanism with two level error detection capability, both for the packet level and for the byte level. During reception, burst noise can affect the communication channel, so that a frame check sum is used to detect excessive errors. In many cases, impulsive noise may cause unpredictable data loss without modifying the frame check sum. Therefore, each byte is transmitted and received in an asynchronous mode inside a 11-bit type word including a start bit, one stop bit, and an odd parity bit to ensure byte integrity.

VIII.1.1 - Frame Format (see Figure 41)

Each frame consists of a preamble, a header, a house address, a link control, a source address, a destination address, a data block, and a frame check sum.

The preambule is 8-bit field with a fixed value FFh: it trains the FSK demodulator, allows a good uart synchronisation for next character. The header consists of a 8-bit pattern AAh chosen with a low probability of wrongly detecting noise or preamble as the header. On a message reception, a matching test is run on the house address field to overcome perturbations coming from a neighbouring home network.

VIII.2 - Use of the ST90E28 resources

- The Watchdog/Timer :
  The watchdog mode is disabled and the timer is operated in continuous mode.
  On each timer interrupt request, network access parameters, keyboard delay time, common system clock parameters are updated. Besides, the ST7537 watchdog input is reset.
- The Serial Communication Interface (SCI) :
  The SCI is configured in asynchronous mode to exchange data between the power line modem and the microcontroller. Every character sent (or received) by the SCI has the following format: 1 start bit, 8 data bits, 1 parity bit (odd parity selected), 1 stop bit. The transmit rate is 1200 bauds.
  To start transmitting a frame, the transmitter buffer register is loaded with the preambule value FFh in order to run the SCI. Each data byte end of transmission results in the generation of an TXHEM (transmitter buffer empty) interrupt request to load the next transmit data byte.
  An outstanding character search is performed to detect the header of an incoming frame (see Figure 42). This is achieved by comparing each received data byte to the content of the data compare register. If the incoming character matches, an RXA (receiver address match) interrupt is requested to enable the analysis of the next data frame fields. Every time the reception of a data byte is completed, a RxD (receive data) interrupt request is generated to store the received data byte.

Figure 40 : Frame Fields

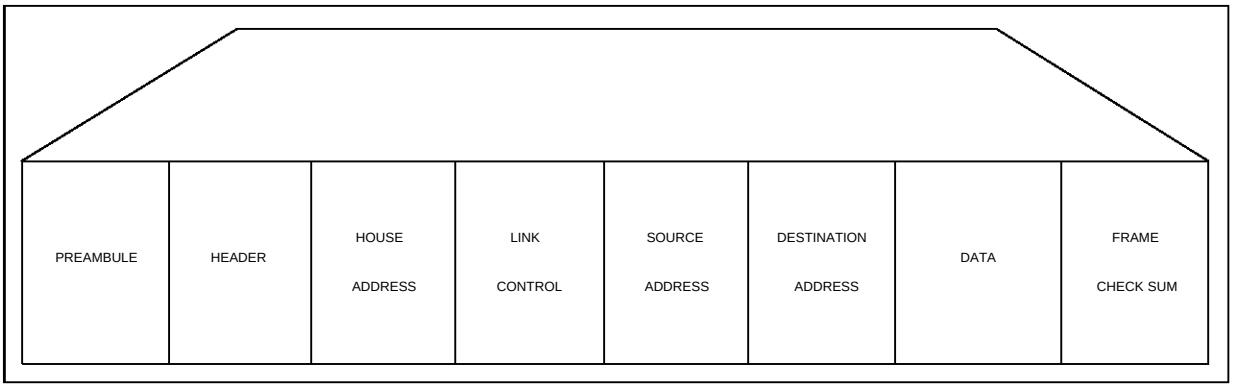
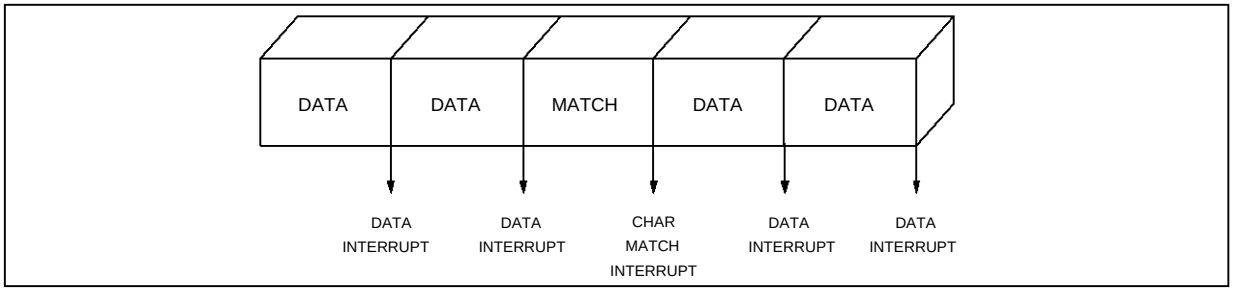
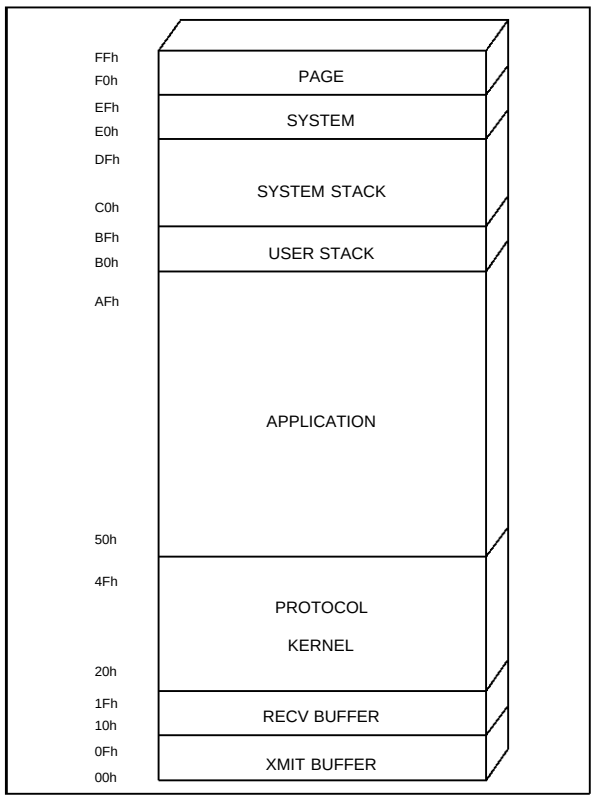


Figure 42 : Character Search Function



- The Register File (see Figure 43) :
  Among the 224 available global purpose registers, 16 registers are reserved as a transmit frame buffer, another group of 16 registers is reserved as a receive frame buffer, 48 registers are dedicated to the protocol kernel, and another group of 48 registers is allocated to the system & user stacks, which leaves 96 registers for storage of applicative values.
- The Input/Output Ports :
  Two of the port pins must be used for the Rx/$\overline{\text{Tx}}$ (P5.0) and $\overline{\text{WD}}$ (P5.1) output signals. Four must be initialized as alternate function for the RSTO (P2.0), $\overline{\text{CD}}$ (P2.4), RxD (P3.6) and TxD (P3.7) signals. Details concerning the initialization of these ports are given in next section.

Figure 43 : Register File Map



VIII.2.1 - Initialization of ST90E28 core and on-chip peripherals

- Core initialization : The user and system stacks are set up in the internal register file. The internal clock frequency is set to 11.0592MHz. The priority level of the main program is set to 7 (lowest), whereas the non-maskable interrupt (RSTO signal) has the top level priority.
- Initialization of the Input/Output ports : Only six input/outputs are required to exchange data between the ST7537 and the ST90E28. The corresponding pins are initialized as follows :

  NMI (Port 2 bit 0) → Alternate function, open drain, TTL
  $\overline{\text{CD}}$ (Port 2 bit 4) → AF, OP, TTL
  RxD (Port 3 bit 6) → AF, OP, TTL
  TxD (Port 3 bit 7) → Alternate function, Push pull, TTL
  Rx/$\overline{\text{Tx}}$ (Port 5 bit 0) → Output, Push pull, TTL
  $\overline{\text{WD}}$ (Port 5 bit 1) → OUT, PP, TTL

  The NMI pin is programmed rising edge sensitive, whereas the CD/ input signal triggers an external interrupt request on a falling edge (INT1 pin) with a priority level set to 1.

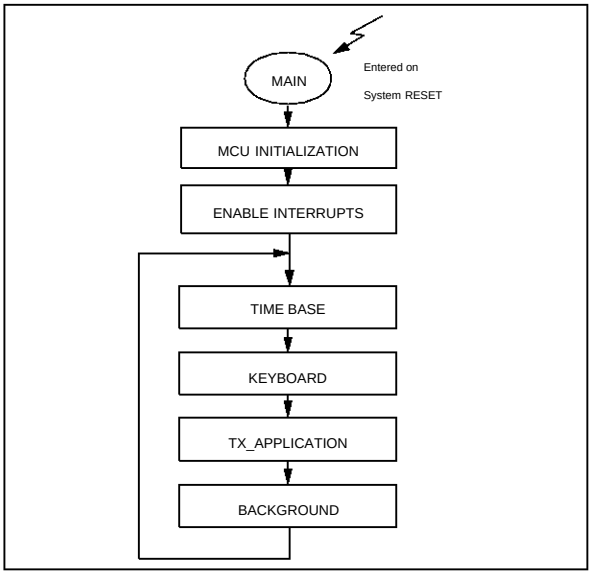
  As for the applicative features, each port pin is initialized as follows :
  display pin → Output, push pull, TTL
  keyboard pin → Input, tristate, TTL
- Timer : The watchdog mode is disabled. Continuous mode is selected with count down from a fixed value of 767, each underflow resulting in an interrupt request and reload of the fixed initial counter value. The internal clock rate, prescaler and initial count value are chosen to give an interrupt request every 555.56µs (1.8kHz = 36*50Hz = 30*60Hz). The timer counter is loaded with the value 767 to complete an end of count every 555.56µs. On each counter underflow an interrupt request (INT0) is generated with a priority level set to 0 (high).
- Serial Communication Interface : The asynchronous mode is selected. The serial interface programmed characteristics are : 8-bit word length,

odd parity generation and detection, 1 stop bit generation, AAh header search. In this mode, each data bit is sampled 16 times, so that each data bit period will be 16 SCI clock periods long. The counter of the baud rate generator is loaded with the fixed value 576 to set the SCI clock rate to 16*1200 = 19200 bauds. The priority level of all SCI interrupts (RXA, RxD, TXHEM) is set to 1.

VIII.2.2 - Main Program

The main is automatically entered on system reset, and first initializes the internal clock, stacks, ports, register file, serial communication interface, and timer. Then the timer starts counting down towards zero from an initial value of 767. Each time the counter clears to zero, an high priority interrupt request will be generated, which will initiate an update of the network access parameters.
The main program loops around the main modules.

Figure 44 : Main Program Flow Chart



ANNEXE A : DEMOBOARD OUTPUT IMPEDANCE

Figure 45

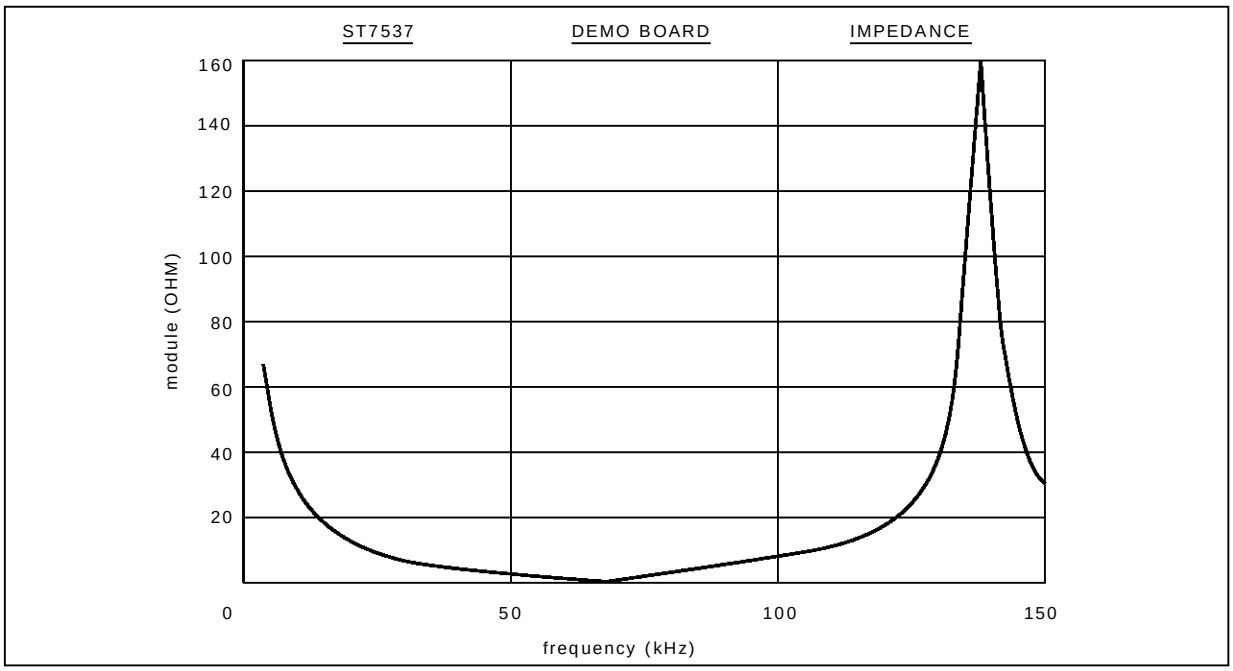
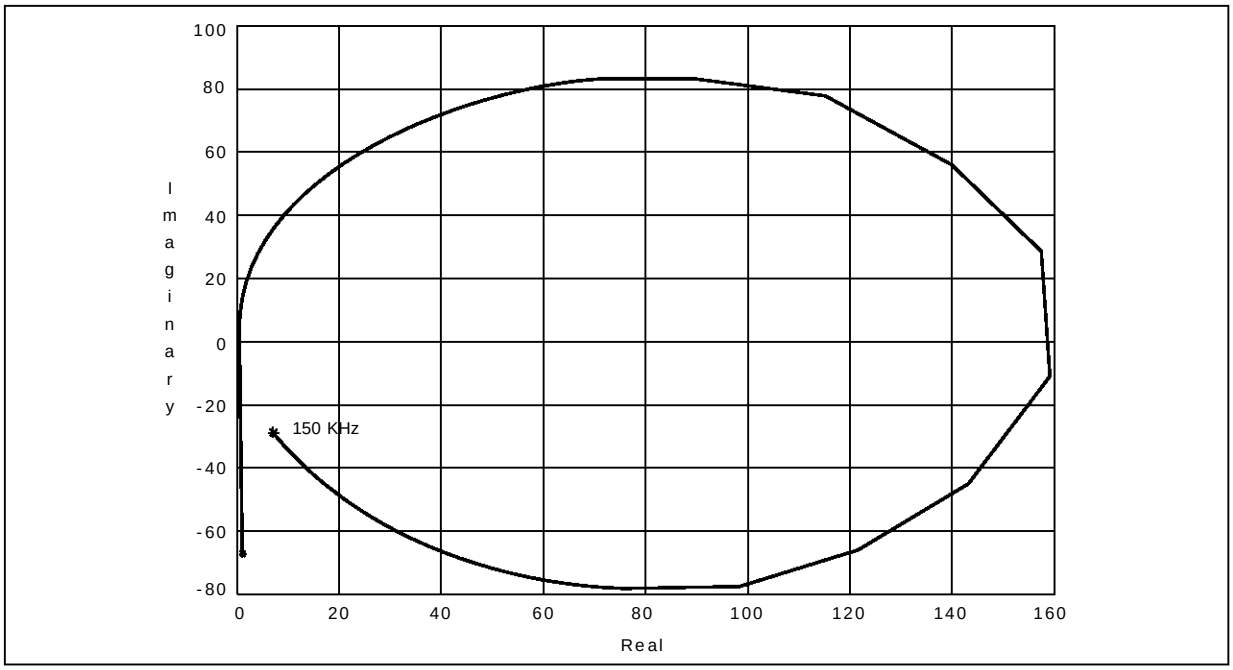


Figure 46



ANNEXE B : DEMOBOARD SCHEMATICS & LAY OUT

Figure 47 : Application Board 7537 DEMO1

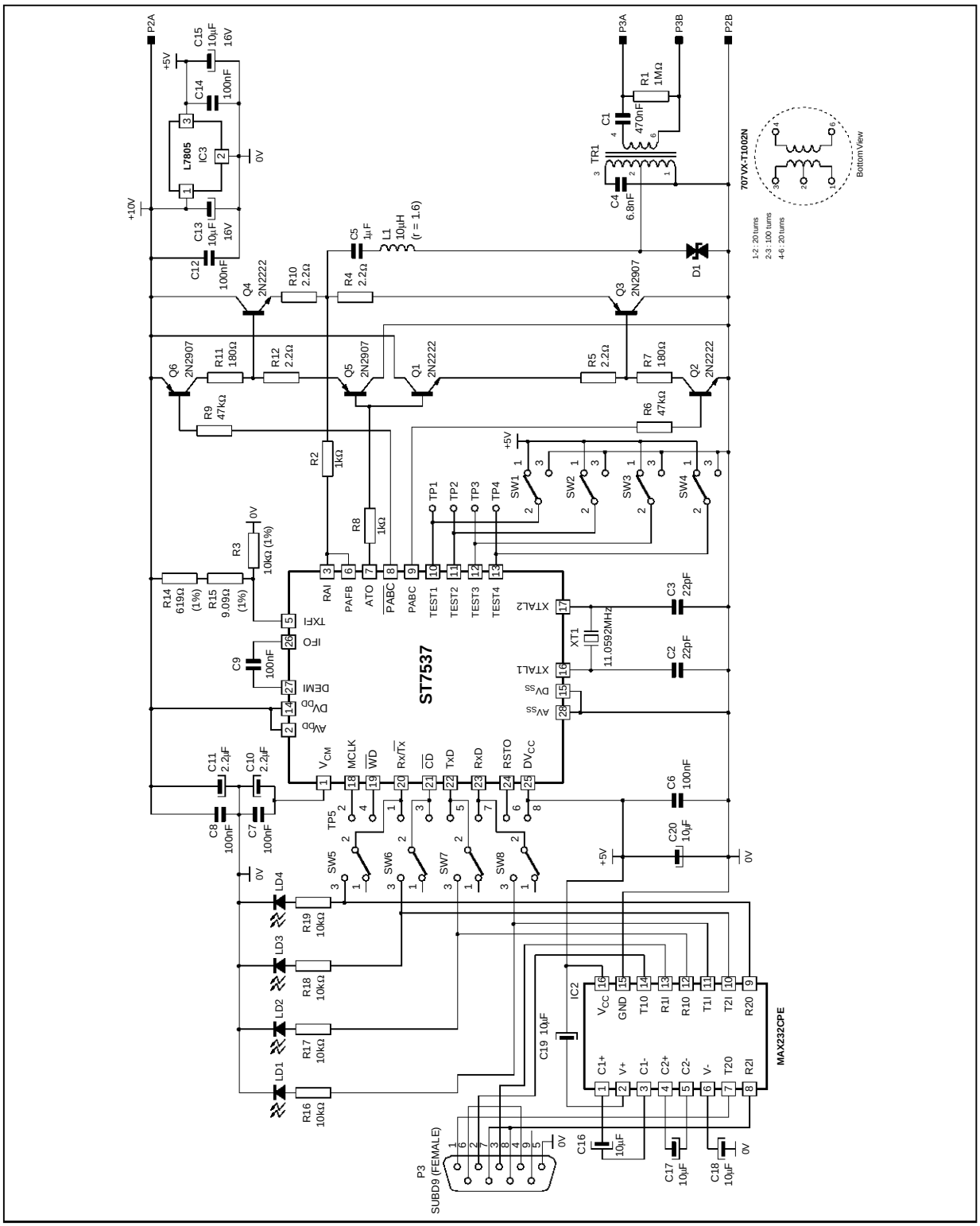
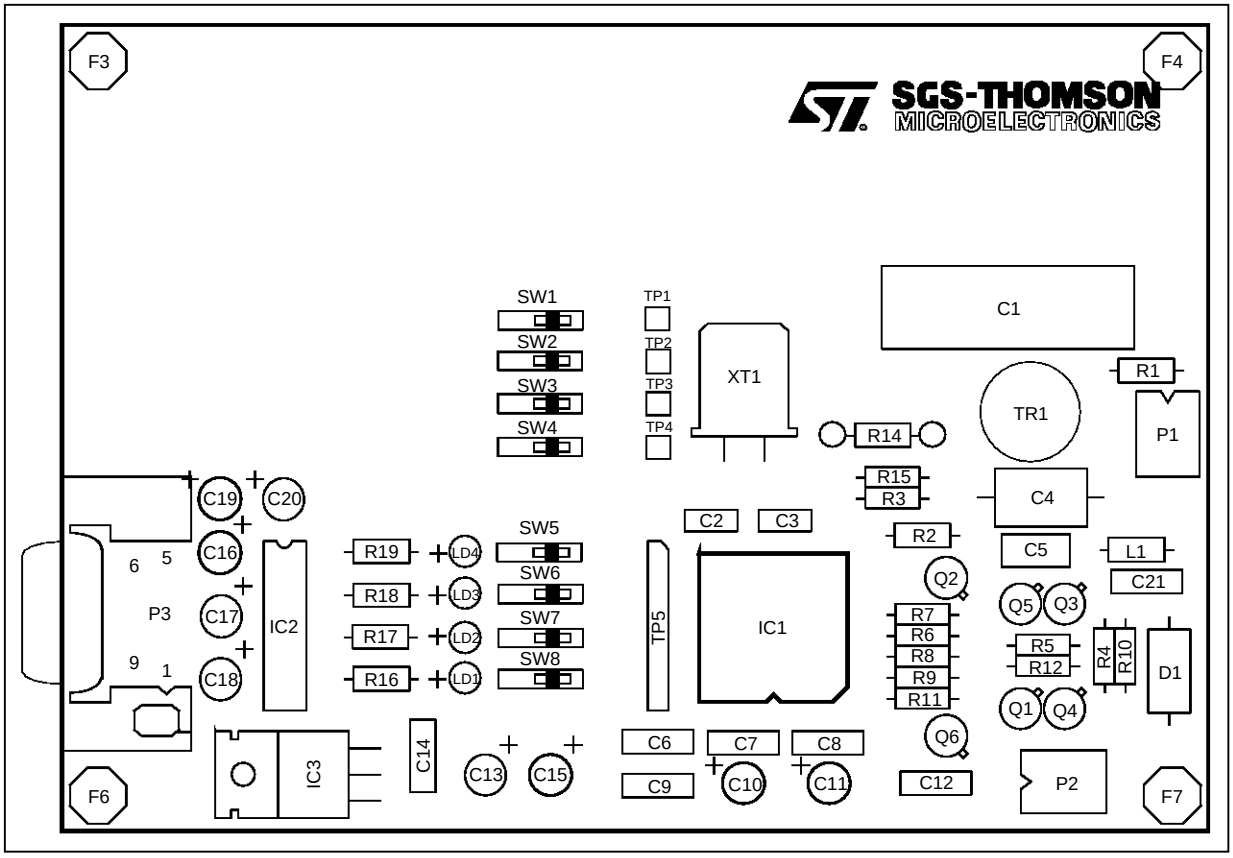


Figure 48 : Layout



Bill Of Materials

Item	Qty.	Reference	Part
1	2	C11,C10	2.2µF
2	6	C7,C6,C8,C9,C12,C14	100nF
3	4	LD4,LD1,LD2,LD3	LED
4	1	IC1	ST7537
5	8	SW8, SW1, SW2, SW3, SW4, SW5, SW6, SW7	
6	1	XT1	CRYSTAL
7	2	R8, R2	1kΩ
8	2	R6, R9	47kΩ
9	3	Q2, Q1, Q4	2N2222
10	3	Q3, Q5, Q6	2N2907
11	1	C4	6.8nF
12	1	C1	470nF
13	1	R1	1MΩ
14	4	R4, R5, R10, R12	2.2Ω
15	2	R11, R7	180Ω
16	1	IC2	MAX232CPE
17	1	IC3	LM7805

Item	Qty.	Reference	Part
18	1	R14	619 (1%)
19	4	R19, R16, R17, R18	10kΩ
20	5	C16, C17, C18, C19, C20	10µF
21	1	C21	15nF
22	2	PICO1, PICO2	PICO
23	2	C13, C15	10nF/16V
24	1	L1	10µH (r=0.8)
25	1	D1	DIODE
26	5	TP2, TP1, TP3, TP4, TP5	POINT
27	1	P3	SUBD9 (FEMALE)
28	1	P2	ALIM
29	1	P1	ALIM+
30	1	TR1	TOKO
31	1	R15	9.09kΩ (1%)
32	1	R3	10kΩ (1%)
33	2	C2, C3	22pF
34	1	C5	1µF

Figure 49 : Master Configuration Board

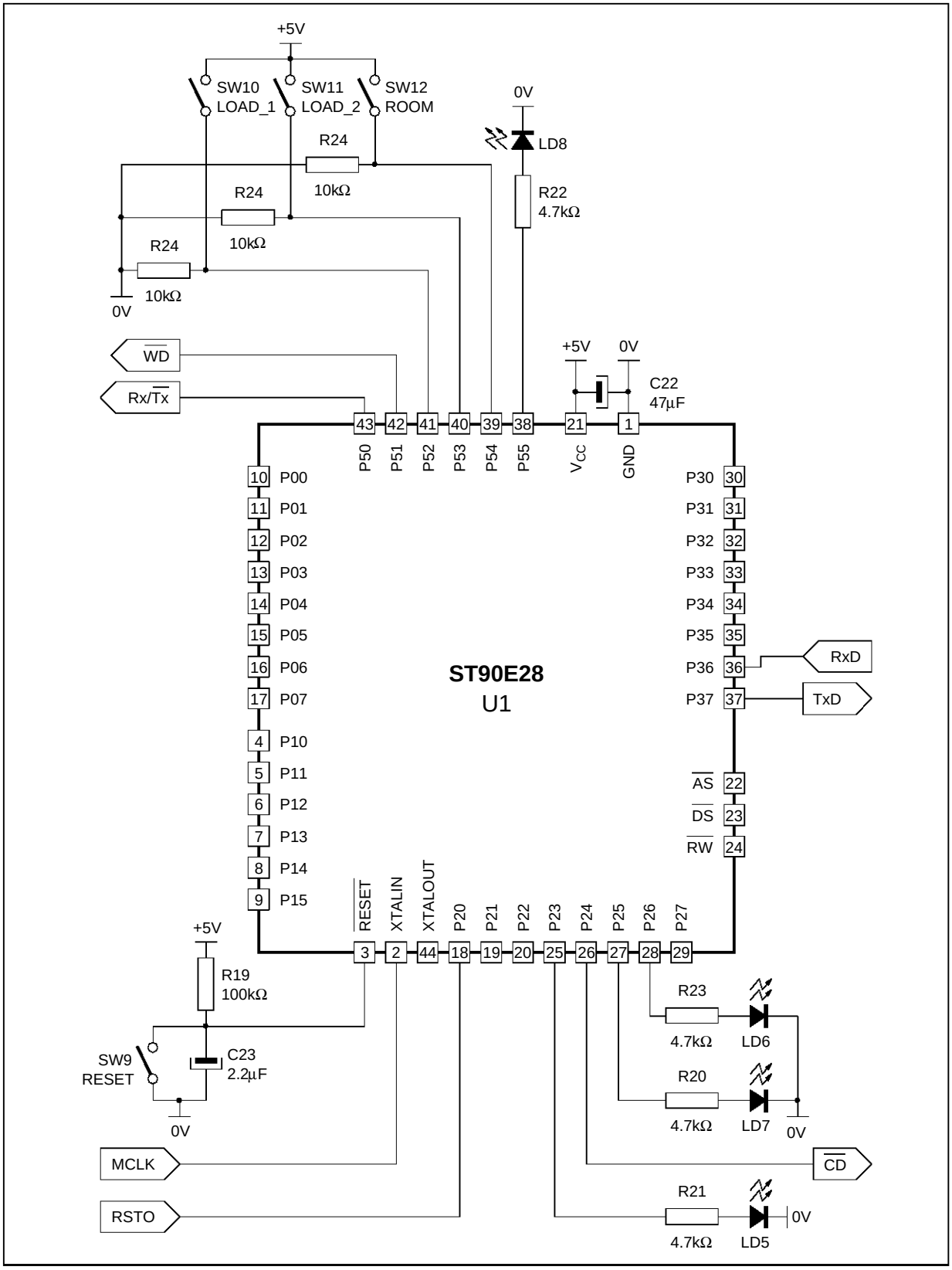
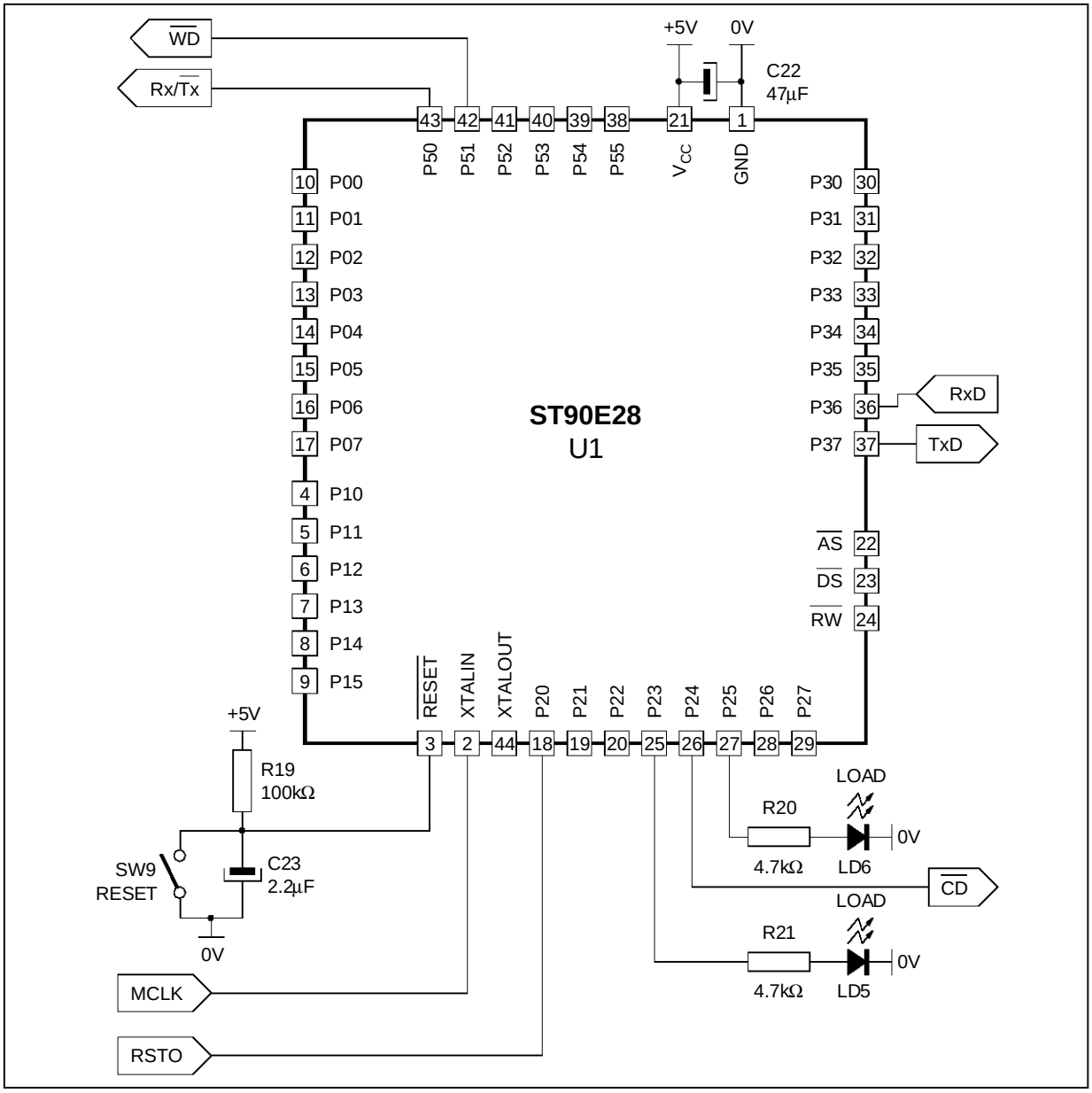


Figure 50 : Slave Configuration Board



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