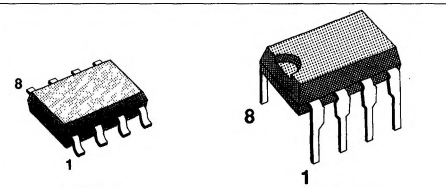
SGS-THOMSON MICROELECTRONICS

ST93C46A

1 K BITS (64x16 or 128x8) SERIAL ACCESS CMOS EEPROM MEMORY

PRELIMINARY DATA

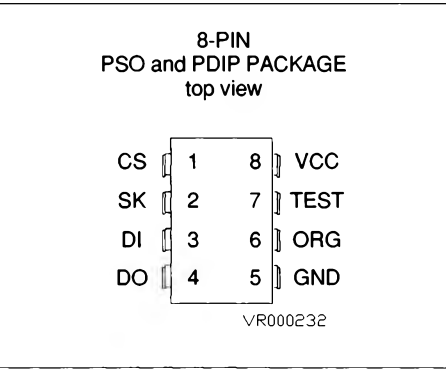
- HIGHLY INCREASED RELIABILITY OF CMOS EEPROM TECHNOLOGY.
- OVER 1 MILLION ERASE/WRITE CYCLES.
- OVER 10 YEARS DATA RETENTION.
- 64 X 16 OR 128 X 8 MEMORY FORMAT USER SELECTABLE.
- WORD AND CHIP PROGRAMMING MODE.
- SELF TIMED PROGRAMMING CYCLE WITH AUTOERASE.
- READY/BUSY SIGNAL IN PROGRAMMING MODE.
- SINGLE POWER SUPPLY IN ALL MODES (5V +/- 10%).
- SEQUENTIAL REGISTER READ.



PSO8 **PDIP8**

(Ordering information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION :

The ST93C46A is a 1024 bits non volatile memory fabricated using SGS-THOMSON highly reliable CMOS EEPROM technology. It is an external memory accessed via a simple serial interface.

The 1K bits memory capacity is divided in either 64 registers of 16 bits each or 128 registers of 8 bits each. The default memory organization is 64 by 16 but it can be switched to 128 by 8 thanks to the "ORG" pin.

The read instruction loads the address of the first register to be read into an 8 bits address pointer. Then the data is clocked out serially on the "D_O" pin. Since the address pointer automatically shifts to the following register address, it's possible, if the "CS" is held high, to produce a serial data stream. In that case, the entire memory can be read in one continuous data stream or as registers of varying length from 16 to 1024 bits. Thus the ST93C46A can be viewed as a non volatile shift register.

In programming mode, the ST93C46A do not require an erase cycle prior to the write instructions. All programming cycles are completely self timed for simplified operations. The standard "write" cycle allows to write 16 bits (resp 8 bits) at a time into one of the 64 (resp 128) data registers.

Following the initiation of a programming cycle, the Ready/Busy status of the chip is available on the "D_O" pin if "CS" is brought high.

PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
D_I	SERIAL DATA INPUT
D_O	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
ORG	ORGANIZATION SELECTION INPUT
GND	GROUND
TEST	THIS PIN IS FOR SGS-THOMSON INTERNAL USE ONLY

A special internal feature of the ST93C46A, "Power on data protection", allows to inhibit all operating modes if Vcc is too low. This feature is particularily useful when powering up the chip.The design of the ST93C46A and its processing with a highly reliable technology yields to typical endurance over 1 million cycles and data retention greater than 10 years.

MEMORY ORGANIZATION :

The ST93C46A is organized, by default, in 64 X 16. Thanks to the ORG pin this organization can be changed. If the ORG pin is connected to Vcc or left unconnected the ST93C46A will stay in the 64 by 16 organization. If the ORG pin is conected to ground, the 128 by 8 organization is selected.

POWER ON DATA PROTECTION :

During power up, all modes of operations are inhibited until Vcc has reached a level between 2.5 and 3.5 v. Reciprocally all modes were inhibited if Vcc falls below the voltage range 2.0 to 3.0 v.

OPERATING MODES :

The ST93C46A has 7 instructions as described in table 1. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 2 bits carry the OP code and the following 6 bits (respectively 7 bits in 128 by 8 organization) the address for register selections.

READ

The read (READ) instruction outputs serial data on the D_O pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16 bits (resp. 8 bits) out shift register. A dummy bit (logical 0) precedes the 16 (resp. 8 bits) data output string.. Output data changes are initiated by a low to high transition of the SK clock. The memory automatically cycles to the next register after 16 data bits (resp. 8 bits) are clocked out as long as CS is held high.

Thus if CS is not brought low (stop condition), the device is in the NON VOLATILE SHIFT REGISTER mode of operation. In this mode, the dummy bit is suppressed and a continuous string of data is obtained.

ERASE / WRITE ENABLE (EWEN)

All programming modes must be preceded by an Erase/Write Enable instruction. Once an Erase/Write enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or Vcc is removed from the part.(Note that after a powering up, the part is in the Erase/Write Disable state).

ERASE / WRITE DISABLE (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disable all programming modes and should follow all programming operations. Execution of a Read instruction is independent of both the EWEN and EWDS instructions.

ERASE (ERASE)

The Erase instruction is a programming instruction which sets all bits of the specified register to the logical "1" state. After the last address bit has been loaded, CS is brought low and this falling edge initiates the self timed programming cycle. The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs" (see section on Ready/Busy status).

WRITE (WRITE)

The Write instruction is followed by 16 (respectively 8) bits of data to be written into the specified address. After the last bit of data is clocked in on the data-in (D_I) pin, CS must be brought low before the next rising edge of the SK clock.This falling edge of CS initiates the self-timed programming cycle.

The D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs" (see section on Ready/Busy status).

ERASE ALL (ERAL)

This instruction is provided to erase the whole chip. With this instruction, each bit of all registers in the memory array is set to the logical "1" state.This programming cycle works in the same way as the ERASE cycle.

WRITE ALL (WRAL)

This instruction is provided to program simultaneously all registers with the data pattern specified in the instruction. All the registers must be erased before doing a WRAL operation; Then, the WRITE ALL programming instruction works in the same way as the WRITE instruction.

READY / BUSY STATUS

During every programming cycle (Erase, Write, Erase all, Write all), the D_O pin indicates the Ready/Busy status of the chip if CS is brought high after a minimum of "Tcs". D_O = logical "0" indicates that the programming is still in progress. D_O = logical "1" indicates that the register at the address specified in the instruction (or all the memory array for ERAL and WRAL instructions) have been programmed, and the part is ready for another instruction. If the part is "ready", the logical "1" on the D_O pin will disappear as soon as the start bit of a new instruction is loaded on the D_I pin.

COMMON I/O SIGNAL

D_I and D_O pins can be connected together. However some precautions should be taken; Therefore it's advised to refer to the SGS-THOMSON application note : "Serial EEPROM Memories : A design guide for common I/O Application".

NOTE ABOUT PIN "TEST"

This pin doesn't affect the device functionality and it is reserved for SGS-THOMSON internal use. For the user, this pin can be either left unconnected or connected to any voltage between Vss and Vcc (Vss and Vcc included).

TABLE 1 : INSTRUCTION SET FOR ST93C46A, ORGANIZATION : 64 x 16

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	COMMENTS
READ	1	10	A_5-A_0		Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXX		Erase/Write enable must precede all programing modes.
EWDS	1	00	00XXXX		Disables all programming instructions.
ERASE	1	11	A_5-A_0		Erase register defined by the specified address.
WRITE	1	01	A_5-A_0	D_{15}-D_0	Writes registers.
ERAL	1	00	10XXXX		Erase all registers.
WRAL	1	00	01XXXX	D_{15}-D_0	Write all registers.

TABLE 2 : INSTRUCTION SET FOR ST93C46A, ORGANIZATION : 128 x 8 ("ORG" PIN CONNECTED TO GND)

INSTRUCTION	SB	OP CODE	ADDRESS	DATA	COMMENTS
READ	1	10	A_6-A_0		Reads data stored in memory, starting at specified address.
EWEN	1	00	11XXXXX		Erase/Write enable must precede all programing modes.
EWDS	1	00	00XXXXX		Disables all programming instructions.
ERASE	1	11	A_6-A_0		Erase register defined by the specified address.
WRITE	1	01	A_6-A_0	D_7-D_0	Writes registers.
ERAL	1	00	10XXXXX		Erase all registers.
WRAL	1	00	01XXXXX	D_7-D_0	Write all registers.

Figure 1 : ST93C46A Block diagram

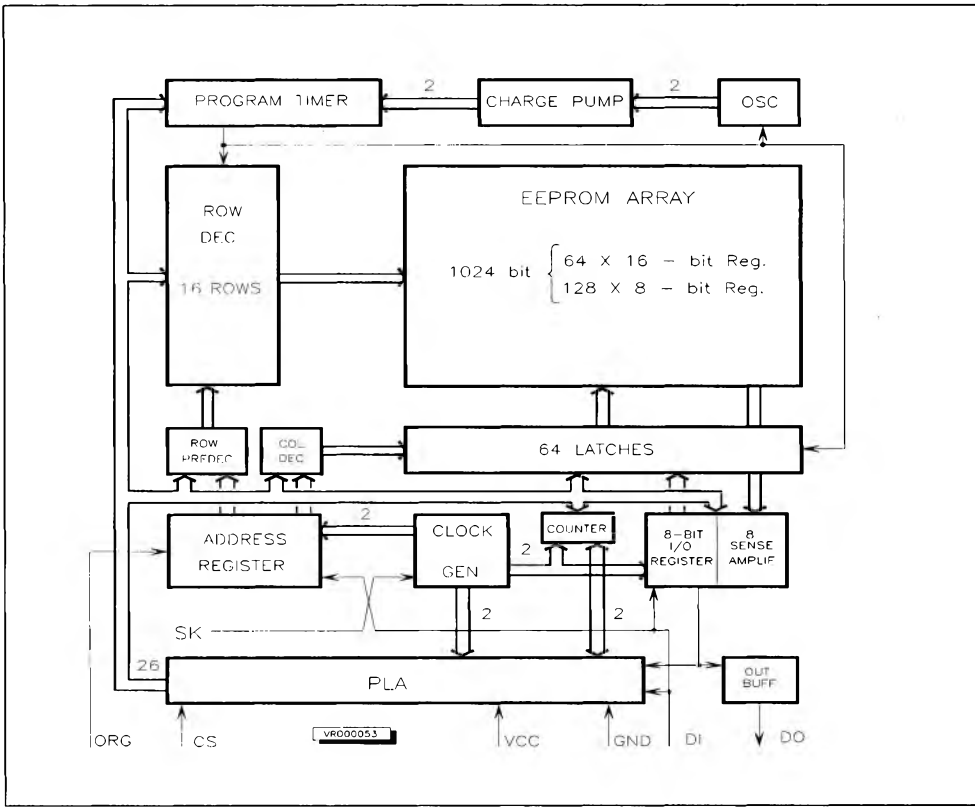


Figure 2 : Synchronous Timing

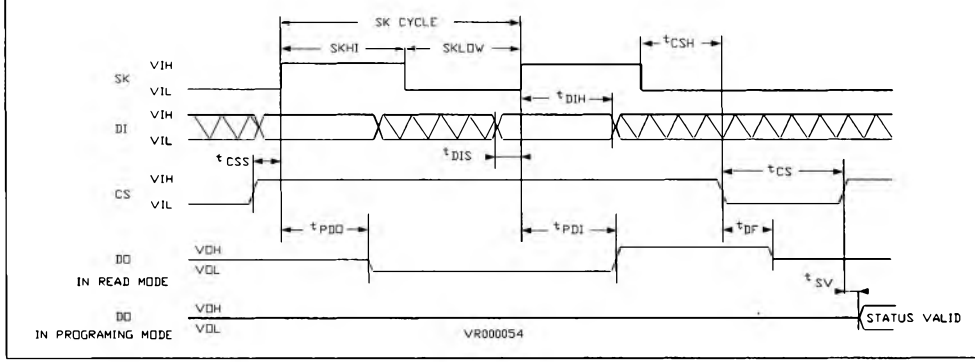


Figure 3 : READ

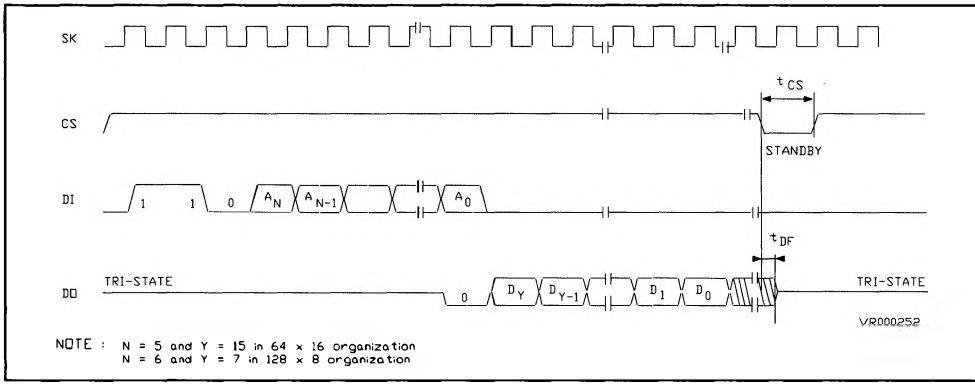


Figure 4 : WRITE

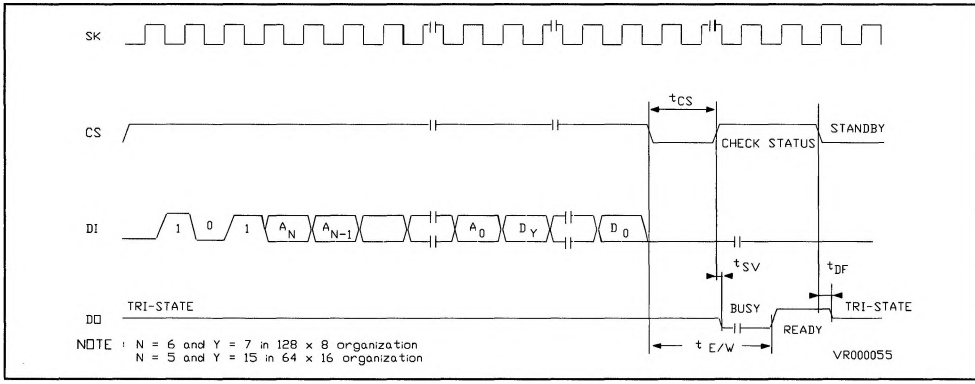


Figure 5 : EWEN/EWDS

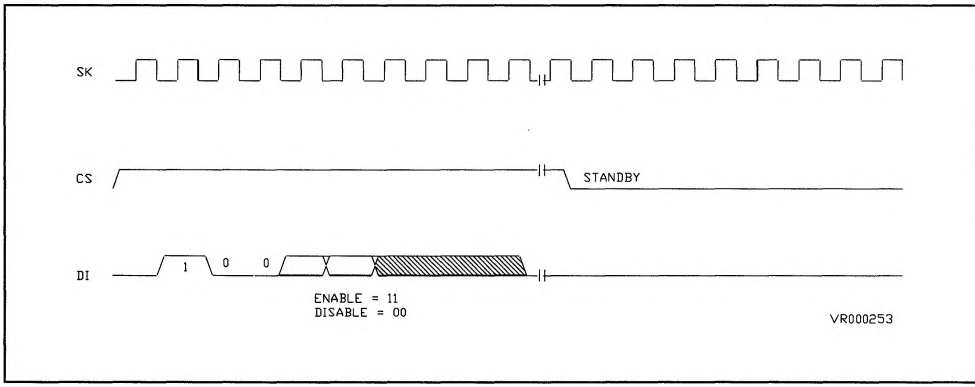


Figure 6 : ERASE

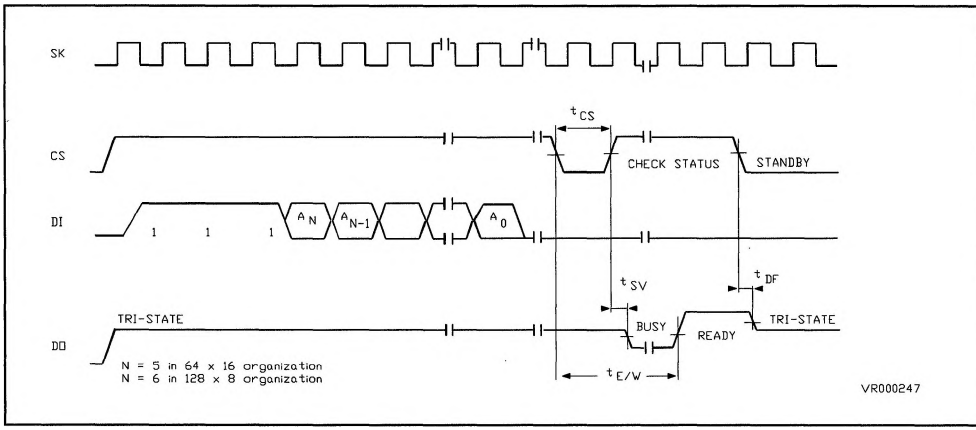


Figure 7 : ERAL

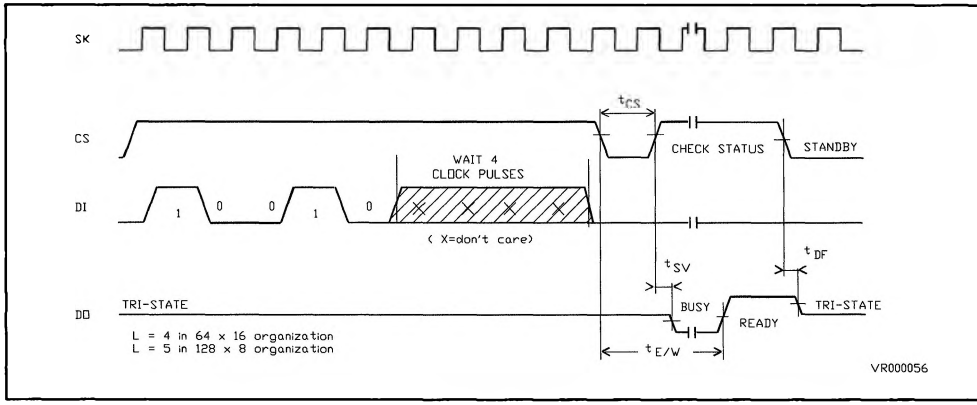
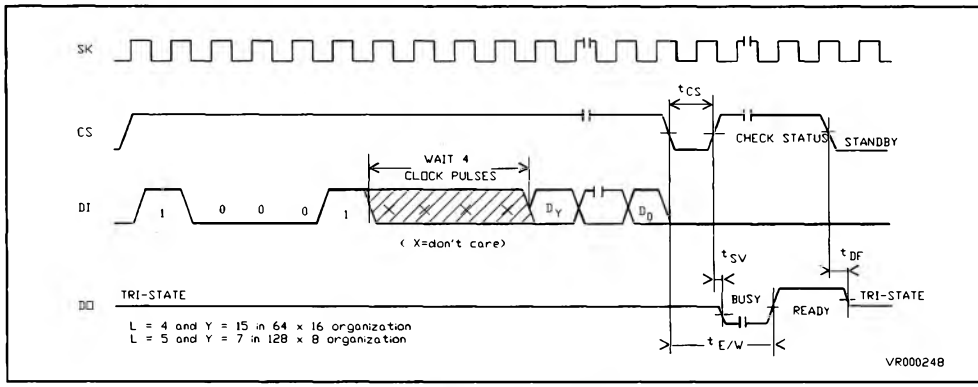


Figure 8 : WRAL



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Ambient storage temperature -65°C to +150°C

All input or output voltage whith respect to ground -0.3v to + 6.5v

Lead Temp (Soldering, 10 sec.) +300°C MAX.

ESD rating 2000v MAX.

DC & AC Electrical characteristics Vcc = 5v +/- 10% (unless otherwise specified)

OPERATINGS CONDITIONS

Ambient operating temperature

ST93C46A *1 0°C to +70°C

ST93C46A *6 -40°C to + 85°C

ST93C46A *3 -40°C to +125°C

Positive power supply 4.5v to 5.5v

* = B = Dual in line package

* = M = SO8 package

CAPACITANCE(note 6) (TA = 25°C, f = 1 Mhz)

SYMBOL	TEST	TYP	Max	Units
COUT	Output Capacitance		5	pF
CIN	Input Capacitance		5	pF

AC Test Conditions

Output Load 1TTL gate and CL= 1OOpF

Input Pulse Levels 0.4v to 2.4v

Timing mesurement Reference level

Input 1v and 2v

Ouput 0.8v and 2v

NOTE 1 : Stress above those listed under " Absolute Maximum ratings " may cause permanent dammage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2 : The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle tSKH + tSKL must be greater or equal to 1microsecond. For example if tSKL = 250 ns then the minimum tSKH = 750 ns in order to meet the SK frequency specification.

3 : The SK frequency specification for extended temperature specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle tSKH + tSKL must be greater or equal to 2 microseconds. For example tSKL = 500 ns then the minimum tSKH = 1.5 Microsecond in order to meet the SK frequency specification.

4 : For commercial parts : CS must be brought low for a minimum of 250ns (tCS) between consecutive instruction cycles.

5 : For extended temperature : CS must be brought for a minimum of 500ns (tCS) between consecutive instruction cycles.

6 : This parameter is periodically sampled and not 100 % tested.

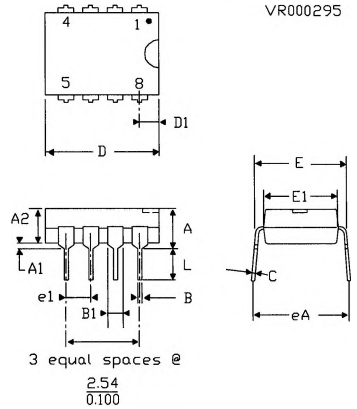
SYMBOL	PARAMETER	PART NUMBER	CONDITIONS	MIN	MAX	UNITS
I_{CC1}	OPERATING CURRENT	ST93C46A*1	CS=VIH,SK=1MHZ		2	mA
	CMOS INPUT LEVELS	ST93C46A*6	SK=0.5MHZ		2	mA
		ST93C46A*3	SK=0.5MHZ		2	mA
I_{CC2}	OPERATING CURRENT	ST93C46A*1	CS=VIH,SK=1MHZ		3	mA
	TTL INPUT LEVELS	ST93C46A*6	SK=0.5MHZ		3	mA
		ST93C46A*3	SK=0.5MHZ		4	mA
I_{CC3}	STANDBY CURRENT	ST93C46A*1	CS=0V		50	uA
		ST93C46A*6			100	uA
		ST93C46A*3			100	uA
I_{IL}	INPUT LEAKAGE	ST93C46A*1	VIN=0V TO VCC	-2.5	2.5	uA
		ST93C46A*6		-10	10	uA
		ST93C46A*3		-10	10	uA
I_{OL}	OUTPUT LEAKAGE	ST93C46A*1	VOUT=0V TO VCC	-2.5	2.5	uA
		ST93C46A*6		-10	10	uA
		ST93C46A*3		-10	10	uA
V_{IL}	INPUT LOW VOLTAGE			-0.1	0.8	V
V_{IH}	INPUT HIGH VOLTAGE			2	VCC+1	V
V_{OL1}	OUTPUT LOW VOLTAGE		IOL =2.1 mA		0.4	V
V_{OH1}	OUTPUT HIGH VOLTAGE		IOH = - 400 uA	2.4		V
V_{OL2}	OUTPUT LOW VOLTAGE		IOL =10 uA		0.2	V
V_{OH2}	OUTPUT HIGH VOLTAGE		IOH = - 10 uA	VCC-0.2		V
f_{SK}	SK CLOCK FREQUENCY	ST93C46A*1		0	1	
		ST93C46A*6		0	0.5	MHZ
		ST93C46A*3		0	0.5	
t_{SKH}	SK HIGH TIME	ST93C46A*1	(Note 2)	250		
		ST93C46A*6	(Note 3)	500		nS
		ST93C46A*3	(Note 3)	500		
t_{SKL}	SK LOW TIME	ST93C46A*1	(Note 2)	250		
		ST93C46A*6	(Note 3)	500		nS
		ST93C46A*3	(Note 3)	500		
t_{CS}	MINIMUM CS	ST93C46A*1	(Note 4)	250		
	LOW TIME	ST93C46A*6	(Note 5)	500		nS
		ST93C46A*3	(Note 5)	500		
t_{CSS}	CS SETUP TIME	ST93C46A*1	Relative to SK	50		
		ST93C46A*6		100		nS
		ST93C46A*3		100		
t_{CSH}	CS HOLD TIME		Relative to SK	0		nS
t_{DIS}	DI SETUP TIME	ST93C46A*1	Relative to SK	100		
		ST93C46A*6		200		nS
		ST93C46A*3		200		
t_{DIH}	DI HOLD TIME	ST93C46A*1	Relative to SK	100		
		ST93C46A*6		200		nS
		ST93C46A*3		200		
t_{PD1}	Output Delay to "1"	ST93C46A*1	AC Test		500	
		ST93C46A*6			1000	nS
		ST93C46A*3			1000	
t_{PD0}	Output Delay to "0"	ST93C46A*1	AC Test		500	
		ST93C46A*6			1000	nS
		ST93C46A*3			1000	
t_{SV}	CS to STATUS VALID	ST93C46A*1	AC Test		500	
		ST93C46A*6			1000	nS
		ST93C46A*3			1000	
t_{DF}	CS to DO in	ST93C46A*1	AC Test		100	
	TRI-STATE	ST93C46A*6	CS = VIL		200	nS
		ST93C46A*3			200	
t_{WP}	Write Cycle TIME				10	mS

ORDERING INFORMATION

PART NUMBER	MAX FREQUENCY	SUPPLY VOLTAGE	TEMP. range	package
ST93C46AB1	1 Mhz	5v +/- 10 %	0° to + 70°C	PDIP8
ST93C46AB6	0.5 Mhz	5v +/- 10 %	- 40° to + 85°C	PDIP8
ST93C46AB3	0.5 Mhz	5v +/- 10 %	- 40° to + 125°C	PDIP8
ST93C46AM1	1 Mhz	5v +/- 10 %	0° to + 70°C	PSO8
ST93C46AM6	0.5 Mhz	5v +/- 10 %	- 40° to + 85°C	PSO8
ST93C46AM3	0.5 Mhz	5v +/- 10 %	- 40° to + 125°C	PSO8

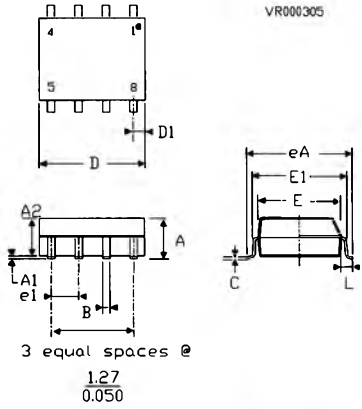
PACKAGE MECHANICAL DATA

PDIL8 PACKAGE (B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1	0.51			0.20		
A2						
B	.356		.550	0.014		0.022
B1	1.15		1.65	0.045		0.065
C	0.204		0.50	0.008		0.020
D			10.92			0.430
D1			1.60			0.063
E						
E1			7.10			0.280
eA	7.95		9.75	0.313		0.384
L		3.30	3.81		0.130	0.150

PSO8 PACKAGE (M)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			.069
A1	0.10			.004		.010
A2			1.65			.065
B	0.35		0.48	.014		.019
C	0.19		0.25	.007		.010
D	4.80		5.00	.189		.197
D1			0.60			.024
E	3.80		4.00	.150		.157
E1						
eA	5.80		6.20	.228		.244
e1		1.27			.050	
L	0.40		1.27	.016		.050