12-Bit, 31-MSPS, Dual-Channel CCD ANALOG FRONT-END FOR DIGITAL COPIERS

FEATURES

- **Dual-Channel CCD Processing:**
  - **Correlated Double Sampler (CDS)**
  - **Sample-and-Hold Mode (S/H)**
  - **Digital Programmable Amplifier**
  - **CCD Offset Correction (OB Loop)**
- **High-Performance ADC:**
  - **12-Bit Resolution**
  - **INL: ±2 LSB**
  - **DNL: ±0.5 LSB**
  - **No Missing Codes Ensured**
- **High-Speed Operation:**
  - **Sample Rate: 31 MHz (max, Design Ensured)**
  - **78-dB SNR (at 0-dB Gain)**
- **Low-Power Consumption:**
  - **Low Voltage: 3.0 V to 3.6 V**
  - **Low Power: 290 mW (typ at 3.3 V)**
  - **Standby Mode: 20 mW (typ)**

APPLICATIONS

- **Copiers**
- **Scanners**
- **Facsimiles**

DESCRIPTION

The VSP5010 is a complete application-specific standard product (ASP) for charge-coupled device (CCD) line sensor applications such as copiers, scanners, and facsimiles. The VSP5010 provides two independent line-processing channels, and performs analog front-end (AFE) data processing and analog-to-digital conversion. Each channel features correlated double sampling (CDS) and sample-and-hold (S/H) processing stages, 14 analog-to-digital converter (ADC) blocks, a digital programmable gain amplifier (DPGA), and an optical black (OB) correction loop. Data are output in a 12-bit word; two-channel ADC data are multiplexed and then output.

The VSP5010 operates from a single 3.3-V supply. The device is available in an LQFP-64 package.

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VSP5010PM	LQFP-64	PM	–25°C to +85°C	VSP5010PM	VSP5010PM	Tray, 160 Pieces
					VSP5010PMR	Tape and Reel, 1000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VSP5010	UNIT
Supply voltage	VCC, VDD	+4.0	V
Supply voltage differences	VCC, VDD	±0.1	V
Ground voltage differences	AGND, DGND	±0.1	V
Digital input voltage		–0.3 to (VDD + 0.3)	V
Analog input voltage		–0.3 to (VCC + 0.3)	V
Input current (all pins except supplies)		±10	mA
Ambient temperature under bias		–40 to +125	°C
Storage temperature		–55 to +150	°C
Junction temperature		+150	°C
Lead temperature (soldering, 5s)		+260	°C
Package temperature (I_R reflow, peak, 10s)		+235	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

		MIN	NOM	MAX	UNIT
Analog supply voltage	VCC	3	3.3	3.6	V
Digital supply voltage	VDD	3	3.3	3.6	V
Analog input voltage, full-scale (0 dB)			1		
Digital input logic family			CMOS		
Digital input clock frequency	System clock	10		30	MHz
Digital output load capacitance			30		pF
Operating free-air temperature, T_A		–25		+85	°C

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP5010PM MIN	TYP	MAX	UNIT
RESOLUTION						
Resolution				12		Bits
SIGNAL PASS						
Signal pass				2		Channels
MAXIMUM CONVERSION RATE						
Maximum conversion rate				30		MHz
DIGITAL INPUT						
Input voltage	V_{T+}	Positive-going threshold		1.8		V
	V_{T-}	Negative-going threshold		1.1		V
Input current	I_{IH}	Logic high, V_{IN} = +3 V			±20	µA
	I_{IL}	Logic low, V_{IN} = 0 V			±20	µA
Input limit			–0.3		VCC + 0.3	V
SYSCLK clock duty cycle				50	%	
Input capacitance				5		pF
DIGITAL OUTPUT (Even Channel and Odd Channel)						
Logic family				CMOS		
Logic coding				Straight Binary		
Multiplexing frequency			60			MHz
Output voltage	V_{OH}	Logic high, I_{OH} = –2 mA	2.5			V
	V_{OL}	Logic low, I_{OL} = 2 mA			0.4	V
ANALOG INPUT (CCDIN)						
Input level for full-scale output		DPGA gain = 0 dB	1400			mV
Allowable feed-through level				1.0		V
Input capacitance				15		pF
Input limit			–0.3		3.6	V
TRANSFER CHARACTERISTICS						
Differential nonlinearity (DNL)		CDS mode = 0 dB, DPGA gain = 0 dB		±0.5	±1	LSB
		SH mode, DPGA gain = 0 dB		±0.5	±1	LSB
Integral nonlinearity (INL)		CDS mode = 0 dB, DPGA gain = 0 dB		±2	±4	LSB
		SH mode, DPGA gain = 0 dB		±4		LSB
No missing codes		DPGA gain = 0 dB		Ensured		
Step input settling time		Full-scale step input		1		Pixel
Overload recovery time		Step input from 2.0 V to 0 V		2		Pixels
Data latency				9 (fixed)		Clocks
Signal-to-noise ratio (1)		DPGA gain = 0 dB		78		dB
		DPGA gain = +24 dB		54		dB
Channel mismatch					±3	%
CORRELATED DOUBLE SAMPLER (CDS)						
Reference level sample settling time		Within 1 LSB, driver impedance = 50 Ω		8.3		ns
Data level sample settling time		Within 1 LSB, driver impedance = 50 Ω		83		ns

(1) SNR = 20 log (16384/output rms noise in LSB), input connected to ground through capacitor.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VSP5010PM MIN	TYP	MAX	UNIT
INPUT CLAMP					
Clamp-on resistance			400		Ω
Clamp level			1.5		V
OB CLAMP LOOP					
CCD offset correction range		–300		300	mV
DAC resolution			10		Bits
Minimum DAC output current	COB pin		±0.15		µA
Maximum DAC output current	COB pin		±153		µA
Loop time constant	C_{COB} = 0.1 µF		40.7		µs
Slew rate	C_{COB} = 0.1 µF, at current DAC full-scale output		1530		V/s
Optical black clamp level	Program range	0		510	LSB
	OB clamp code = 0101 0000b		160		LSB
REFERENCE					
Positive reference voltage			1.85		V
Negative reference voltage			1.1		V
DIGITAL PROGRAMMABLE AMPLIFIER (DPGA)					
Gain program resolution			10		Bits
Gain	Gain code = 11 1111 1111b, 24 dB		16		V/V
	Gain code = 10 0000 0000b, 18 dB		8		V/V
	Gain code = 00 0100 0000b, 0 dB		1		V/V
	Gain code = 00 0000 0000b, —		0		V/V
Gain error			±0.5		dB
SERIAL INTERFACE					
Data length	Chip address = 2 bits, register address = 4 bits, and data = 10 bits		2		Bytes
Serial clock frequency				10	MHz
POWER SUPPLY					
Supply voltage VCC, VDD		3.0	3.3	3.6	V
Power dissipation	VCC = VDD = 3.3 V, f_{SYSCLK} = 30 MHz, load = 10 pF		290		mW
	Standby mode		20		mW
TEMPERATURE RANGE					
Operation temperature		–25		+85	°C
Storage temperature		–55		+125	°C
Thermal resistance θ_{JA}	LQFP-64 package		83		°C/W

PRODUCT PREVIEW

PIN CONFIGURATION

VSP5010PM
LQFP-64
(TOP VIEW)

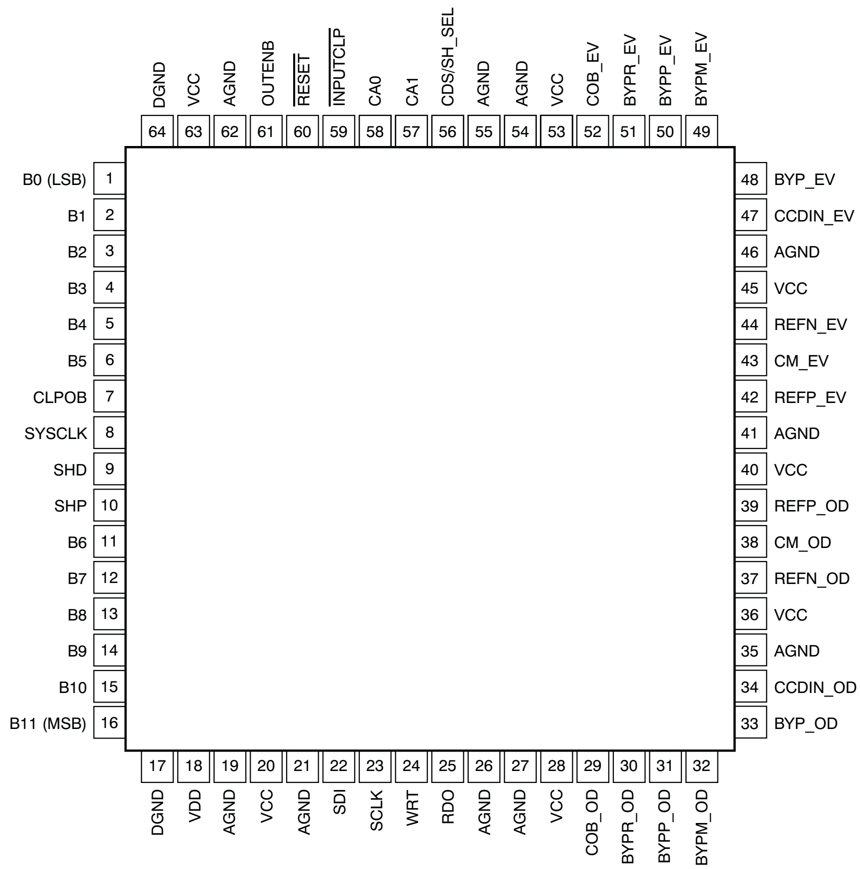


Table 1. TERMINAL FUNCTIONS

TERMINAL		TYPE(1)	DESCRIPTION
NAME	NO.		
B0 (LSB)	1	DO	ADC output, bit 0 (least significant bit)
B1	2	DO	ADC output, bit 1
B2	3	DO	ADC output, bit 2
B3	4	DO	ADC output, bit 3
B4	5	DO	ADC output, bit 4
B5	6	DO	ADC output, bit 5
CLPOB	7	DI	Optical black clamp pulse
SYSCLK	8	DI	System clock input
SHD	9	DI	CCD data sampling pulse
SHP	10	DI	CCD reference sampling pulse
B6	11	DO	ADC output, bit 6
B7	12	DO	ADC output, bit 7
B8	13	DO	ADC output, bit 8
B9	14	DO	ADC output, bit 9
B10	15	DO	ADC output, bit 10
B11 (MSB)	16	DO	ADC output, bit 11 (most significant bit)
DGND	17	P	Digital ground for digital outputs (B0–B11)

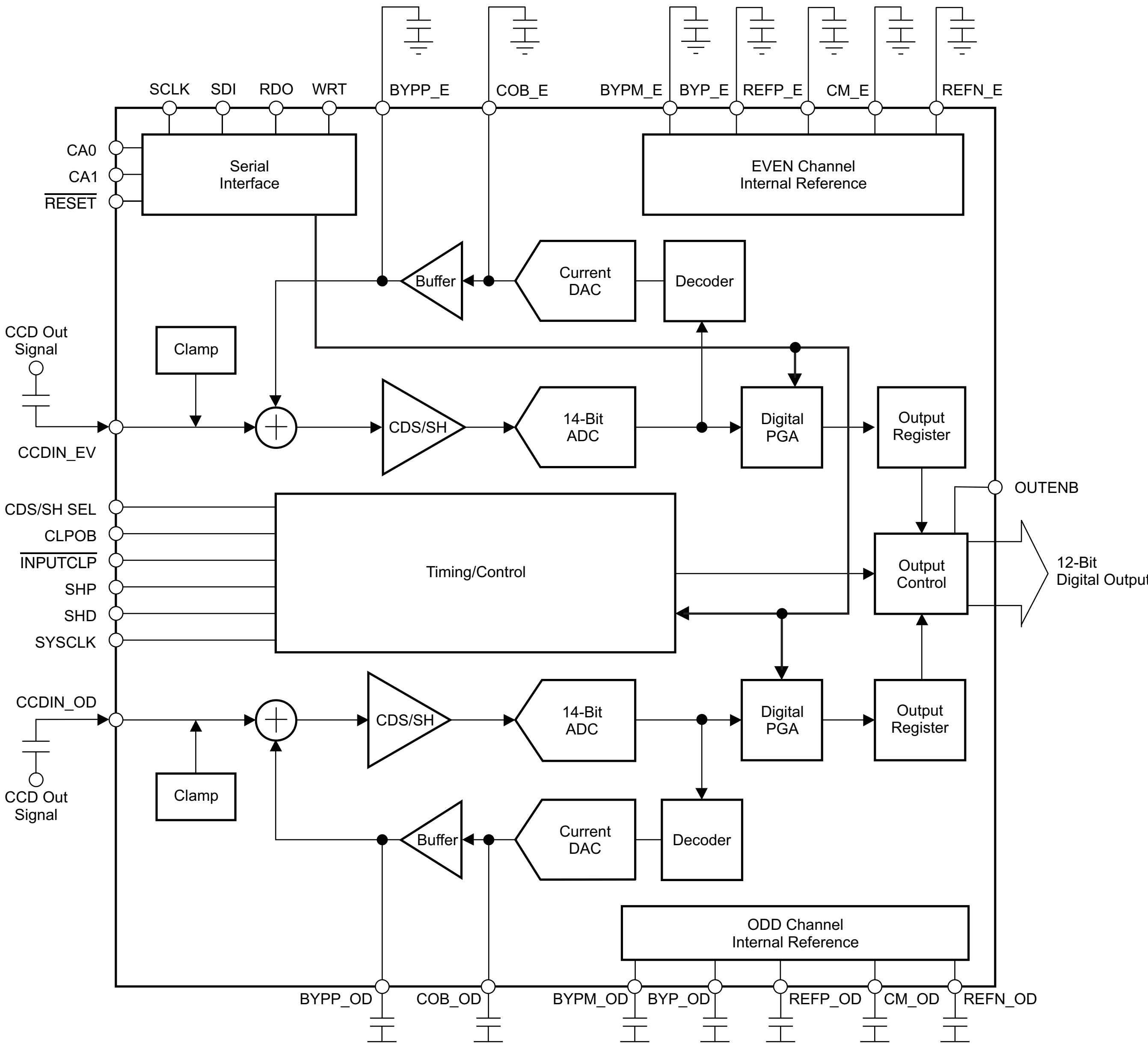
(1) Designators in TYPE: P = power supply and ground; DI = digital input; DO = digital output; AI = analog input; and AO = analog output.

PRODUCT PREVIEW

Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE(1)	DESCRIPTION
NAME	NO.		
VDD	18	P	Digital supply for digital outputs (B0–B11)
AGND	19	P	Analog ground
VCC	20	DI	Analog power supply
AGND	21	DI	Analog ground
SDI	22	DI	Serial interface data input
SCLK	23	DI	Serial interface data shift clock (rising edge trigger)
WRT	24	DI	Serial interface data write pulse (rising edge trigger)
RDO	25	DO	Serial interface register read output
AGND	26	P	Analog ground
AGND	27	P	Analog ground
VCC	28	P	Analog power supply
COB_OD	29	AO	OB loop output voltage (odd); connect 0.1-µF capacitor between ground
BYPR_OD	30	AO	Input buffer reference bypass (odd)
BYPP_OD	31	AO	CDS positive reference bypass (odd); open or bypass to ground by a 0.1-µF capacitor
BYPM_OD	32	AO	CDS negative reference bypass (odd); open or bypass to ground by a 0.1-µF capacitor
BYP_OD	33	AO	CDS common reference bypass (odd); bypass to ground by a 0.1-µF capacitor
CCDIN_OD	34	AI	CCD signal input (odd)
AGND	35	P	Analog ground
VCC	36	P	Analog supply
REFN_OD	37	AO	ADC negative reference bypass (odd); bypass to ground by a 0.1-µF capacitor
CM_OD	38	AO	ADC common reference (odd); bypass to ground by a 0.1-µF capacitor
REFP_OD	39	AO	ADC positive reference (odd); bypass to ground by a 0.1-µF capacitor
VCC	40	P	Analog power supply
AGND	41	P	Analog ground
REFP_EV	42	AO	ADC positive reference bypass (even); bypass to ground by a 0.1-µF capacitor
CM_EV	43	AO	ADC common reference bypass (even); bypass to ground by a 0.1-µF capacitor
REFN_EV	44	AO	ADC negative reference bypass (even); bypass to ground by a 0.1-µF capacitor
VCC	45	P	Analog power supply
AGND	46	P	Analog ground
CCDIN_EV	47	AI	CCD signal input (even)
BYP_EV	48	AO	CDS common reference bypass (even); bypass to ground by a 0.1-µF capacitor
BYPM_EV	49	AO	CDS negative reference bypass (even); bypass to ground by a 0.1-µF capacitor
BYPP_EV	50	AO	CDS positive reference bypass (even); bypass to ground by a 0.1-µF capacitor
BYPR_EV	51	AO	Input buffer reference bypass (even); bypass to ground by a 0.1-µF capacitor
COB_EV	52	AO	OB loop output voltage (even); connect 0.1-µF capacitor between ground
VCC	53	P	Analog power supply
AGND	54	P	Analog ground
AGND	55	P	Analog ground
CDS/SH_SEL	56	DI	CDS/SH mode select; high = CDS mode, low = SH mode
CA1	57	DI	Chip address 1
CA0	58	DI	Chip address 0
$\overline{\text{INPUTCLP}}$	59	DI	Input clamp control (active low)
$\overline{\text{RESET}}$	60	DI	Asynchronous register reset (active low)
OUTENB	61	DI	Output enable/disable; high = high impedance, low = output enable
AGND	62	P	Analog ground
VCC	63	P	Analog power supply
DGND	64	P	Digital ground for digital outputs (B0–B11)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

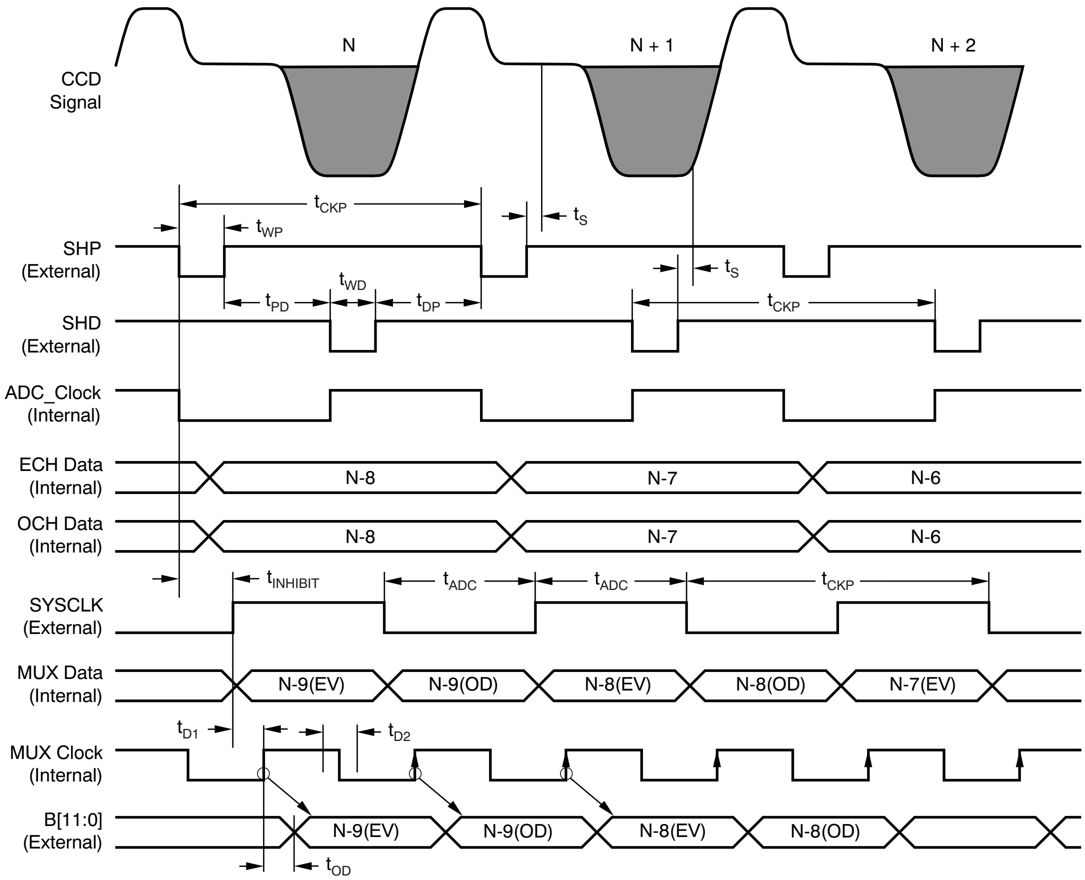


Figure 1. VSP5010 CDS Mode Timing Specifications (Even and Odd Channels) 1

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CKP}	Clock period(1)	32			ns
t_{ADC}	SYSCLK pulse width(2)	16			ns
t_{WP}	SHD pulse width	6	8.3		ns
t_{WD}	SHD pulse width	6	8.3		ns
t_{PD}	SHP trailing edge to SHD leading edge	8			ns
t_{DP}	SHD trailing edge to SHP leading edge	8			ns
t_S	Sampling delay		3.5		ns
$t_{INHIBIT}$	Inhibited clock period	10			ns
t_{D1}	Internal MUX clock delay 1(3)		4		ns
t_{D2}	Internal MUX clock delay 2(3)		4		ns
t_{OD}	Output delay at data output delay = 0 ns(4)		13		ns
	Output delay at data output delay = 2 ns(4)				
DL	Data latency(5)		13		ns

(1) Design ensured. A shipment final test is 33 ns.
(2) Design ensured. A shipment final test is 16.7 ns.
(3) See the *Serial Interface* section.
(4) Load = 25 pF, data output delay = 2 ns indicates that the delay time is set by the Configuration Register of the serial interface. See the *MPX Clock Edge Phase* configuration.
(5) Depending on an *Internal MUX clock delay* and *output delay*, latency can carry out the decrease of an increase.

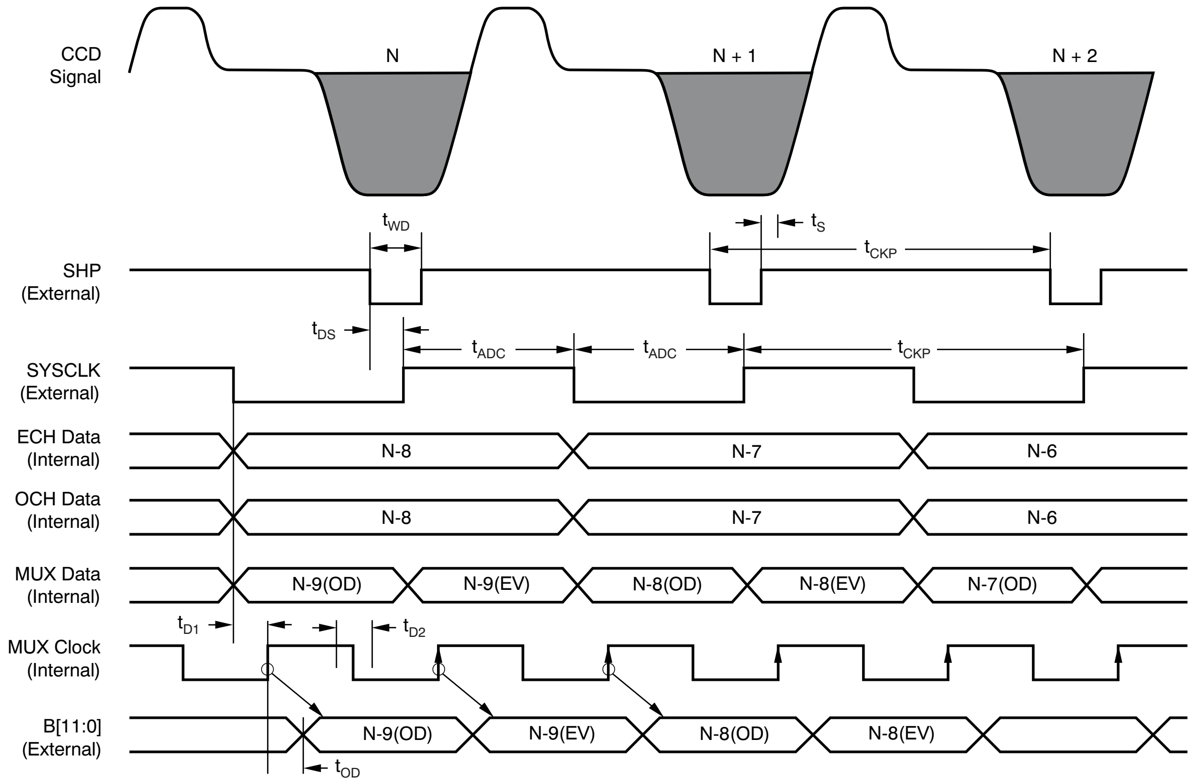


Figure 2. VSP5010 SH Mode Timing Specifications (Even and Odd Channels) 1

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CKP}	Clock period (1)	32			ns
t_{ADC}	SYSCLK pulse width (2)	16			ns
t_{WD}	SHD pulse width	6	8.3		ns
t_S	Sampling delay		3.5		ns
t_{DS}	SHD trailing edge to SYSCLK leading edge	–8		+6	ns
t_{D1}	Internal MUX clock delay 1 (3)		4.5		ns
t_{D2}	Internal MUX clock delay 2 (3)		12.5		ns
t_{OD}	Output delay at data output delay = 0 ns (4)		13		ns
	Output delay at data output delay = 2 ns (5)		17		ns
DL	Data latency		9		Clocks

(1) Design ensured. A shipment final test is 33 ns.
(2) Design ensured. A shipment final test is 16.7 ns.
(3) See the *Serial Interface* section.
(4) Load = 25 pF, data output delay = 0 ns indicates that the delay time is set by the Configuration Register of the serial interface.
(5) Load = 25 pF, data output delay = 2 ns indicates that the delay time is set by the Configuration Register of the serial interface.

PRODUCT PREVIEW

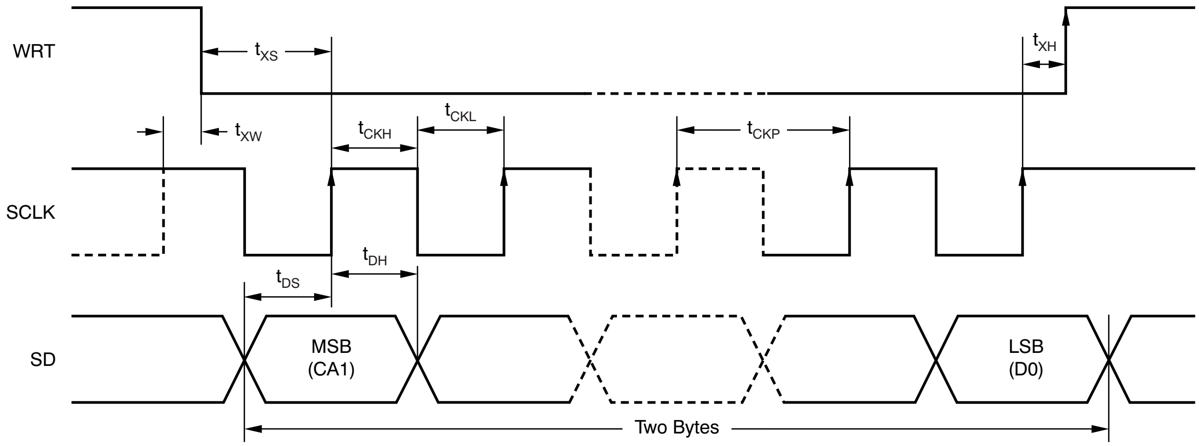


Figure 3. Serial Interface Timing Specification 1

TIMING CHARACTERISTICS (31-MHz Operation)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CKP}	Clock period	100			ns
t_{CKH}	Clock high pulse width	40			ns
t_{CKL}	Clock low pulse width	40			ns
t_{DS}	Data setup time	30			ns
t_{DH}	Data hold time	30			ns
t_{XS}	WRTL to SCLK setup time	15			ns
t_{XH}	SCLK to WRT hold time	15			ns
t_{XW}	WRT setup time	15			ns

PRODUCT PREVIEW

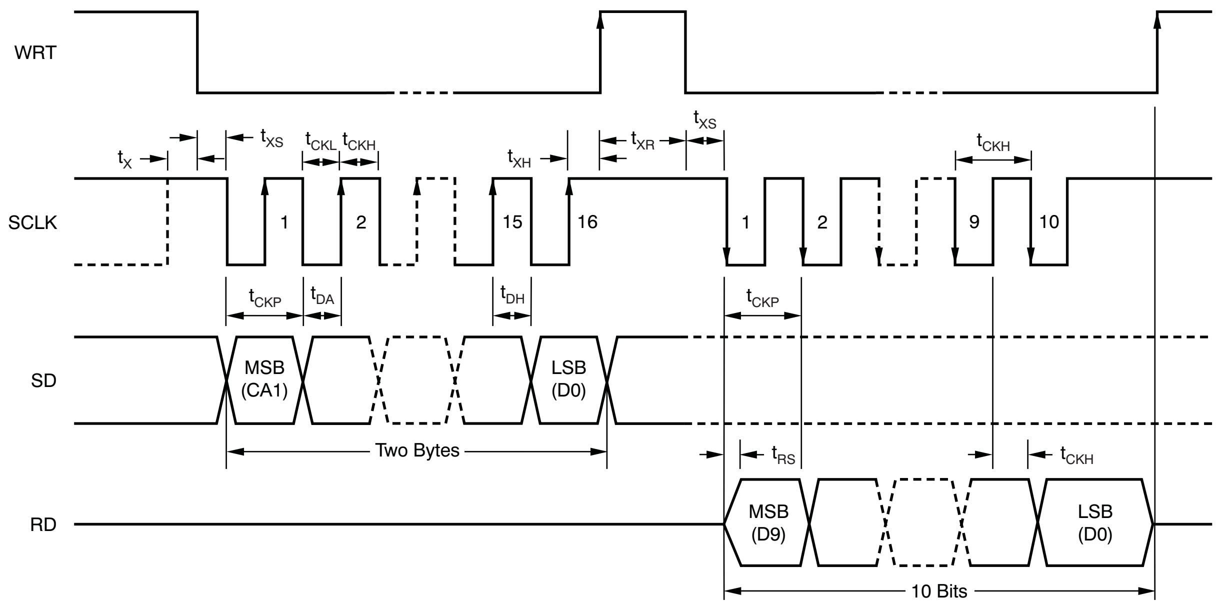


Figure 4. Serial Interface Timing Specification 2 (Read)

TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CKP}	Clock period	100			ns
t_{CKH}	Clock high pulse width	40			ns
t_{CKL}	Clock low pulse width	40			ns
t_{DS}	Data setup time (write)	30			ns
t_{DH}	Data hold time (write)	30			ns
t_{XS}	WRTL to SCLK setup time	15			ns
t_{XH}	SCLK to WRT hold time	15			ns
t_{XW}	WRT setup time	15			ns
t_{WRW}	Minimum WRT width	10			ns
t_{RS}	Data setup time (reading)			30	ns

PRODUCT PREVIEW

APPLICATION INFORMATION

OVERVIEW

The VSP5010 was developed as an analog front-end for charge-coupled device (CCD) line imaging sensor applications such as copiers, facsimiles, and so forth. The VSP5010 provides two independent EVEN/ODD channels for processing, with each channel operating at 31 MHz.

Output signals from each EVEN/ODD channel of the CCD image sensor are sampled at the correlated double sampling (CDS) circuit and then transmitted to a 14-bit, high-precision analog-to-digital converter (ADC). The ADC output is then amplified by the required gain at a digital programmable gain amplifier (DPGA) and then rounded to 12-bit data, and output sequentially as EVEN/ODD data that are synchronized with SYSCLK. The CDS stage can be also used as a sample-and-hold (S/H) step.

Each channel has an optical black level clamp circuit (OB loop) and automatically compensates offsets of the CCD and CDS/SH during the OB pixel period (CLPOB). The OB level output value can be set at a required value through the serial interface. DC bias lost in ac coupling is reproduced as an input clamp voltage, which is the necessary level for internal operation. Input clamp voltage is charged to a capacitor that is connected to CCDIN during a dummy pixel period ($\overline{\text{INPUTCLP}}$) by SHP.

Gain setting, operation polarity of each clock, operating mode selection, and so forth are done through the serial interface by accessing internal registers. Each setting of register values can be reset to its respective default value by setting $\overline{\text{RESET}}$ to active low.

CORRELATED DOUBLE SAMPLER (CDS) AND SAMPLE/HOLD (S/H) CIRCUIT

The CDS circuit removes low-frequency and/or common-mode noise, such as fluctuations per pixel, from the CCD image sensor output. Noises longer than one pixel period among the input signals are rejected by a subtraction operation at the CDS circuit. Figure 5 shows a simplified CDS block diagram.

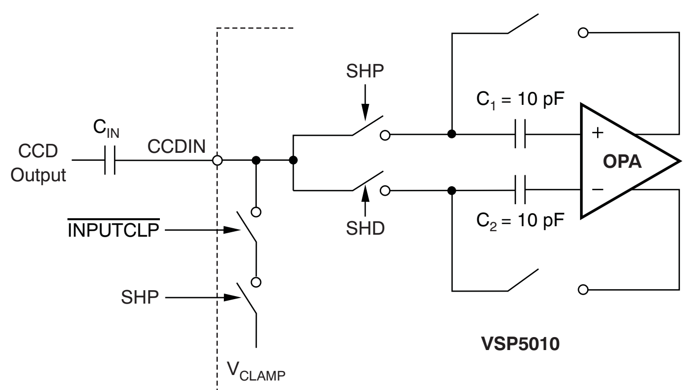


Figure 5. Simplified Block Diagram

The CDS circuit can be configured as a sample-and-hold (S/H) circuit by the CDS/SH SEL pin. A simplified S/H circuit block diagram is shown in Figure 6.

In the S/H mode, the input clamp voltage (V_{CLAMP}) is charged by $\overline{\text{INPUTCLP}}$ and the sampling signal (SHD) to the C_{IN} capacitor. $\overline{\text{INPUTCLP}}$ is activated at the dummy pixel (or OB pixel) of CCD. By these operations, the dummy pixel (or OB pixel) level voltage is fixed to V_{CLAMP} at the CCDIN terminal.

When sampling for the OB pixel and an effective pixel, the V_{CLAMP} voltage is charged to capacitor C_1, and C_2 charges the voltage lower than V_{CLAMP} according to the signal voltage from the CCD. As the voltage difference in C_1 and C_2 is acquired during the hold period, signals from the CCD are acquired as voltage based on V_{CLAMP}.

In CDS mode, the signal voltage is received as the voltage difference between the sampled voltage of SHP (reference level) and SHD (data level); the signal level is not affected even when V_{CLAMP} charges or fluctuates because of leakage, etc. However, when operated as S/H, the V_{CLAMP} fluctuation is read as an offset error because the signal is acquired based on V_{CLAMP}. In order to prevent V_{CLAMP} leakage, a buffer is inserted at the input in S/H mode.

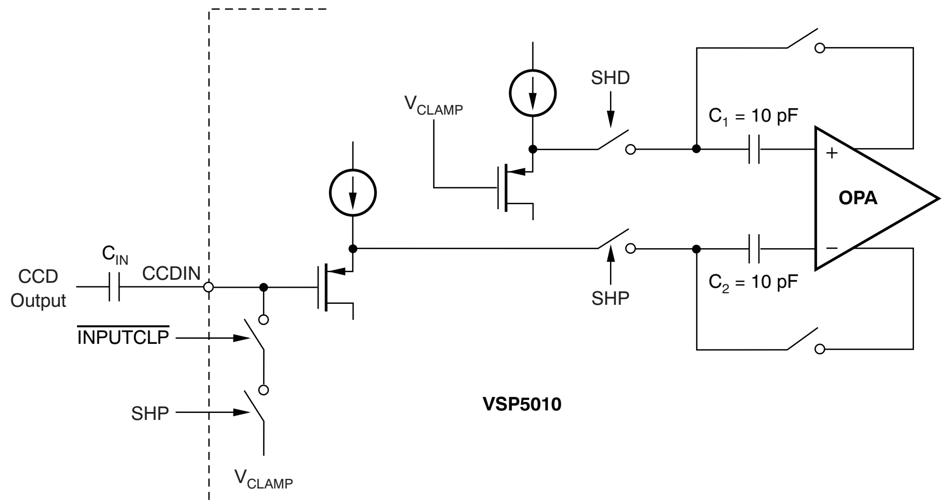


Figure 6. Simplified Sample-and-Hold (S/H) Circuit

INPUT CLAMP (DUMMY PIXEL CLAMP)

Output from the CCD image sensor is ac-coupled with the VSP5010 through a capacitor. The purpose of the input clamp is to reproduce the dc bias lost by ac coupling, and to supply an optimum dc bias for proper device operation at the CDS/SH circuit. Refer to Figure 5 and Figure 6 for simplified block diagrams of the input clamp circuit.

The input signal level is clamped to the internal reference voltage by activating both SHP (during CDS mode; activate SHD during SH mode) and $\overline{\text{INPUTCLP}}$ during the CCD dummy pixel output period.

HIGH PRECISION A/D CAPACITOR

The ADC block of the VSP5010 consists of a pipeline architecture. This converter has a complete differential circuit configuration and error correction circuit, and ensures 14-bit resolution.

Circuits that generate the necessary reference voltage at the ADC are built inside the device, and are shown as REFP (high-potential reference), REFN (low-potential reference), and CM (common-mode voltage) pins outside the device. In order to assure ADC accuracy, these reference voltage pins must be sufficiently decoupled by a capacitor (0.1 μF recommended).

PRODUCT PREVIEW

DIGITAL PROGRAMMABLE GAIN AMPLIFIER (DPGA)

The DPGA circuit can control gain values in the range of 0 V/V to 16 V/V by inputting a digital code through the serial interface. Gain changes linearly in proportion to the code setting, as shown in Figure 7.

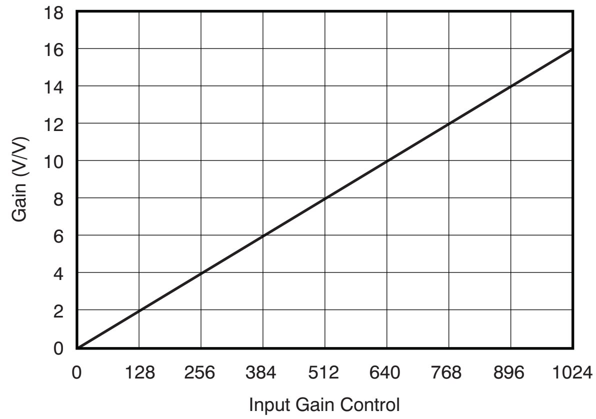


Figure 7. Block Diagram of CDS and Input Clamp

PRODUCT PREVIEW

OPTICAL BLACK LEVEL (OB) LOOP AND OB CLAMP LEVEL

The VSP5010 has a built-in self-calibration circuit (OB loop) that compensates the OB level by using optical black (OB) pixels output from the CCD image sensor. A block diagram of the OB loop and OB clamp circuit is shown in Figure 8.

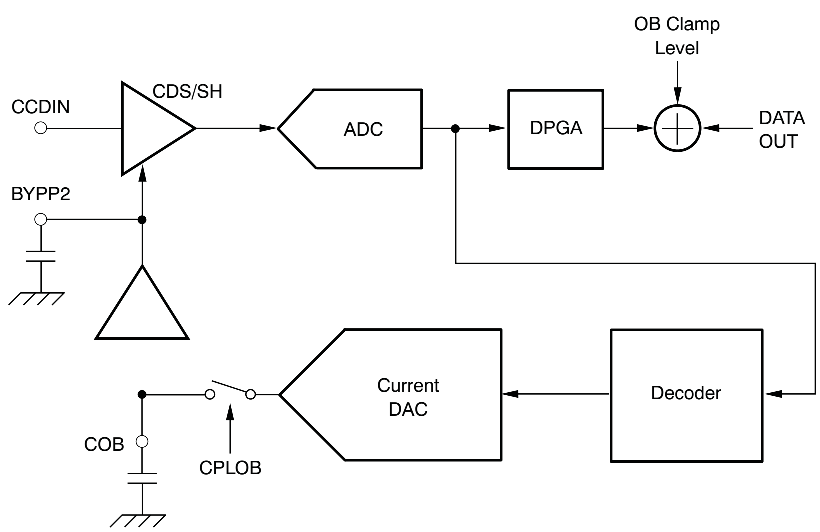


Figure 8. OB Loop and OB Level Clamp

The CCD offset is compensated by converging this calibration circuit while activating CLPOB during a period when OB pixels are output from the CCD.

In CDS mode, CCD offset is compensated as a difference between the reference level and the data level of the OB pixel. In SH mode, V_{CLAMP} is compensated by $\overline{\text{INPUTCLP}}$ as the difference between fixed dummy pixels and the OB pixels.

These compensated signal levels are recognized as actual *OB levels*, and outputs are clamped to OB levels set by the serial interface. These OB levels are the base of black for the effective pixel period thereafter.

The DPGA is a gain stage outside the OB loop; therefore, OB levels are not affected even when the gain changes.

The converging time of the OB loop is determined based on the capacitor value connected to the COB terminal and the output from the current output digital-to-analog converter (DAC) of the loop. The time constant (T) can be obtained from Equation 1:

$$T = C/(16384 \times I_{MIN}) \quad (1)$$

Where:

- C is the capacitor value connected to COB,
- I_{MIN} is the minimum current (0.15 μA) of the current DAC, which has a current equivalent to 1 LSB of the DAC converter output.

When C = 0.1 μF, T is 40.7 μs.

The slew rate (SR) can be obtained from Equation 2:

$$SR = I_{MAX}/C \quad (2)$$

Where:

- C is the capacitor value connected to COB,
- I_{MAX} is the maximum current (153 μA) of the current DAC, which is the equivalent current to 1023 LSB of the DAC converter output.

The OB clamp level (digital output value) can be set externally through the serial interface by inputting a digital code to the OB clamp level register. The digital code to be input and the corresponding OB clamp level are shown in Table 2.

Table 2. Input Code and OB Clamp Level to be Set

CODE	CLAMP LEVEL (LSB) VSP5010 (12-BIT)
0000 0000b	0
0000 0001b	2
—	—
0100 1111b	158
0101 0000 (default)	160
0101 0001b	162
—	—
1011 1111b	508
1111 1111b	510

SETTLING OF OB LOOP AND INPUT CLAMP

Because these capacitors are discharged at start-up and after a long standby state, these two capacitors must be charged to the proper operational voltage.

The charging time for the input clamp voltage is the logical AND of SHP (SHD in S/H mode) and $\overline{\text{INPUTCLP}}$. The actual charging time per line is the duration of the SHP pulse times the number of dummy pixels in the line. Equally, COB is only charged during the OB pixel period. Therefore, some time is necessary to bring the VSP5010 into a normal operating state at device start-up.

Though start-up time depends on the number of dummy and pixels per line, at least 500 ms to 1 s should be allowed.

STANDBY MODE

Normal operation mode and standby mode can be switched by the serial interface.

In standby mode, power consumption can be saved; all operation is suspended other than the interface circuit and reference voltage supply. During standby mode, additional power consumption may be obtained by suspending SYSCLK. When restoring a SYSCLK that was suspended during standby mode, more than two clocks of SYSCLK must be acquired before inputting commands.

PRODUCT PREVIEW

OUTPUT DATA DELAY

Large transient noise occurs when the output data change because several logic lines change simultaneously. When this transient noise timing overlaps the analog signal sampling timing, it may affect the ADC converting value. To avoid this effect, changing the timing of the VSP5010 output data can be delayed in approximately 3-ns steps by serial control.

The delay value set refers to the increase in default time between SYSCLKL and the data output set in the timing specification.

TEST MODE AND TEST PATTERN

The VSP5010 can be set to test mode by setting the configuration register. During test mode, the test pattern generated inside will be output with or without a CCD input signal.

There are two test patterns. One is a pattern which outputs the code that is the OB level +128 LSB for a specified number of pixels (stripe pattern); the other is a pattern which increments the output code from 1 to 4095 by a specified number of LSBs per pixel (gradation pattern). These patterns can be selected by setting the configuration register through the serial interface.

CHIP ADDRESS

The VSP5010 has two chip address pins, CA0 and CA1. Setting these pins gives a particular address for the device, and the data-writing device can be selected by the address in serial interface data. By this function, the serial interface can be used as a common line for up to four devices.

REGISTER READING

Each register data can be read from the RDO pin by setting bit A3 of the serial interface data to '1', and setting the reading register address to A[2:0].

After writing the address to specify which register is to be read, assert WRT and apply SCLK. The value of the register is output sequentially on the RD pin. Refer to the Serial Interface Timing Specification 2 (Read) for details.

While reading registers, the writing function is disabled.

SERIAL INTERFACE REGISTER DESCRIPTION

The serial interface of the VSP5010 is composed of three signals; SDI, SCLK, and WRT. SDI data are sequentially stored to the shift register at the rising edge of SCLK, and shift register data are stored to the parallel latch at the rising edge of WRT.

Serial data are two bytes of fixed length and are composed of a two-bit chip address, a four-bit register address, and 10-bit data. The chip address can only write register to a device that matches its value to the address set by CA0 and CA1. By using this two-bit chip address, the serial interface can be shared by other devices.

Both the address (A[3:0]) and the serial data (D[9:0]) start with the MSB (A3, D9) and end with the LSB (A0, D0). When data with more than two bytes are applied, the final two bytes immediately before the rising edge of WRT are effective, and any data writtenbefore that are lost.

Register configuration and serial data format are shown in Table 3.

Each register value is defined at the time of device power-on (VCC = 2.1 V (typ)).

Table 3. Serial Interface Command Data Format

	MSB															LSB
REGISTERS	**CA1**	**CA0**	**A3**	**A2**	**A1**	**A0**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Configuration	X(1)	X	0	0	0	0	0	0	C7	C6	0	C4	0	C2	C1	C0
Standby mode and Clk Dly	X	X	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	0	S0
DPGA gain EVEN	X	X	0	0	1	0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
DPGA gain ODD	X	X	0	0	1	1	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
OB clamp level EVEN	X	X	0	1	0	0	0	0	O7	O6	O5	O4	O3	O2	O1	O0
OB clamp level ODD	X	X	0	1	0	1	0	0	O7	O6	O5	O4	O3	O2	O1	O0
Test mode	X	X	0	1	1	0	0	0	0	0	T5	T4	0	T2	0	T0
Internal ADCK monitor	X	X	0	1	1	1	0	0	0	0	0	0	0	0	PT1	0
Read out	X	X	1	R2	R1	R0	X	X	X	X	X	X	X	X	X	X

Configuration Register Description (Address = 000h)

Bits C[2:0]	**Clock Polarity**		
	Bit C0 (INPUTCLP Polarity)	**Bit C1 (CLPOB Polarity)**	**Bit C2 (SHP/SHD Polarity)**
	0 = Active low (default) 1 = Active high	0 = Active low (default) 1 = Active high	0 = Active low (default) 1 = Active high
Bit C4	**Data Output Order**		
	0 = EVEN/ODD (default) 1 = ODD/EVEN		
Bits C[7:6]	**Data Output Delay**		
	Bit C7	**Bit C6**	
	0 = Time (0 ns, typ) (default)	0 Delay = time (0 ns, typ) (default)	
	0 = Delay time (2 ns, typ)	1 = Delay time (2 ns, typ)	
	1 = Delay time (4 ns, typ)	0 = Delay time (4 ns, typ)	
	1 = Delay time (6 ns, typ)	1 = Delay time (6 ns, typ)	

(1) X = Don't care.

PRODUCT PREVIEW

PRODUCT PREVIEW

Standby Mode and MPX Clock Edge Phase Description (Address = 01h)

Bit S0	**Standby/Normal Operation Select**
	0 = Normal operation mode (default) 1 = Standby mode
Bits D[8:1]	**MPX Clock Edge Phase**
	Figure 9 illustrates the MPX clock edge phase.
Bits D[5:2]	**Dlyedge 2 Timing (except constant delay t_{D1})**
	0000b = Delay time (1.6 ns)
	1000b = Delay time (8.0 ns) (default, 0.8 ns/step)
	1111b = Delay time (13.6 ns)
Bits D[9:6]	**Dlyedge 1 Timing (except constant delay t_{D1})**
	0000b = Delay time (–2.4 ns)
	1000b = Delay time (0 ns) (default, 0.3 ns/step)
	1111b = Delay time (2.1 ns)

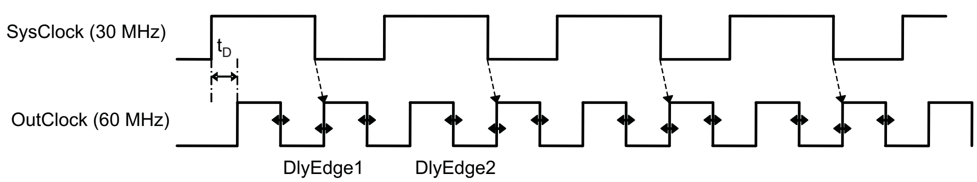


Figure 9. MPX Clock Edge Phase

CAUTION:

Please do not use at Delayedge 1 > Delayedge 2

(example: D[5:2] = 0000b and D[9:6] = 1111b)

Delayedge2 should maintain sufficient width to allow proper data output timing.

Internal ADCK Monitor Description (Address = 07h)

Bit D1	**PT1**
	0 = Normal 1 = Internal ADC clock to B0 (ADC output, bit 0, least significant bit)

EVEN Channel Gain Register Description (Address = 02h)

Bits G[9:0]	**Gain Value**
	GAIN[9:0] /64 (default = 00 0100 0000b)

ODD Channel Gain Register Description (Address = 03h)

Bits G[9:0]	**Gain Value**
	GAIN[9:0] /64 (default = 00 0100 0000b)

EVEN Channel OB Clamp Register Description (Address = 04h)

Bits O[7:0]	**OB Clamp Level**
	2 LSB × O[7:0] (default = 0101 0000b)

ODD Channel OB Clamp Register Description (Address = 05h)

Bits O[7:0]	**OB Clamp Level**
	2 LSB × O[7:0] (default = 0101 0000b)

Test Mode Register Description (Address = 06h)

Bit T0	**Test Mode Enable/Disable**	
	0 = Disable (default) 1 = Enable	
Bit T2	**Test Pattern Select**	
	0 = Gradation pattern (default) 1 = Stripe pattern	
Bits T[5:4]	**Test Pattern Data Interval**	
	Bit T5	**Bit T4**
	0 = Stripe pattern (8 pixels), gradation pattern (2 pixels) (default)	0 = Stripe pattern (8 pixels), gradation pattern (2 pixels) (default)
	0 = Stripe pattern (16 pixels), gradation pattern (4 pixels)	1 = Stripe pattern (16 pixels), gradation pattern (4 pixels)
	1 = Stripe pattern (32 pixels), gradation pattern (8 pixels)	0 = Stripe pattern (32 pixels), gradation pattern (8 pixels)
	1 = Stripe pattern (64 pixels), gradation pattern (16 pixels)	1 = Stripe pattern (64 pixels), gradation pattern (16 pixels)

Register Read Out Description

Bit A[2:0]	**R[2:0]**
	2:0 = Set reading register address

POWER SUPPLY, GROUNDING AND DEVICE DECOUPLING RECOMMENDATIONS

The VSP5010 incorporates a very high-precision and high-speed ADC and analog circuitry which are vulnerable to any extraneous noise from the rails or elsewhere. For this reason, although the VSP5010 has analog and digital supply pins, it should be treated as an analog component; all supply pins except for VDD should be powered by the analog supply only. This configuration ensures the most consistent results, because digital power lines often carry high levels of wideband noise that would otherwise be coupled into the device and degrade the achievable performance.

Proper grounding, short lead length, and the use of ground planes are also very important for high-frequency designs. Multilayer printed circuit boards (PCBs) are recommended for the best performance; these types of boards offer distinct advantages such as minimizing ground impedance, separation of signal layers by ground layers, and so forth. It is highly recommended that analog and digital ground pins of the VSP5010 be joined together at the IC and be connected only to the analog ground of the system.

The driver stage of the digital outputs (B[11:0]) is supplied through a dedicated supply VDD (pin 18) and it should be separated from the other supply pins completely or at least with a ferrite bead.

Because of the high operation speed, the converter also generates high-frequency current transients and noise that are fed back into the supply and reference lines. This additional interference requires the supply and reference pins be sufficiently bypassed. In most cases, 0.1-µF ceramic chip capacitors are adequate to decouple the reference pins. Supply pins should be decoupled to the ground plane with a parallel combination of tantalum (1-µF to 22-µF) and ceramic (0.1-µF) capacitors. The effectiveness of the decoupling depends largely on the proximity to the individual pin. VDD should be decoupled to the proximity of DGND (pin 17 and pin 64).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
VSP5010PM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM	
VSP5010PMG6	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM	
VSP5010PMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM	
VSP5010PMRG6	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	A42 SNBI	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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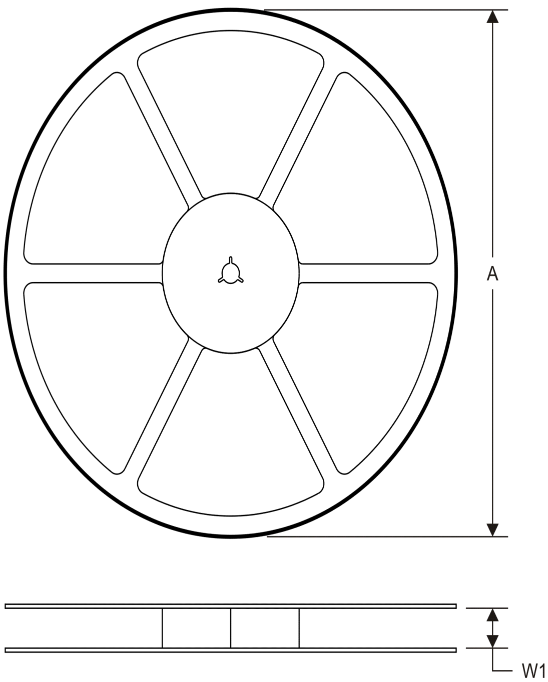
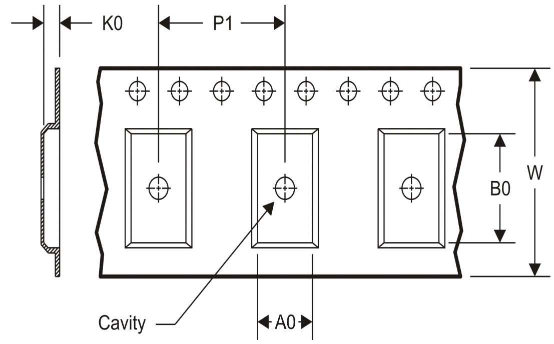
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



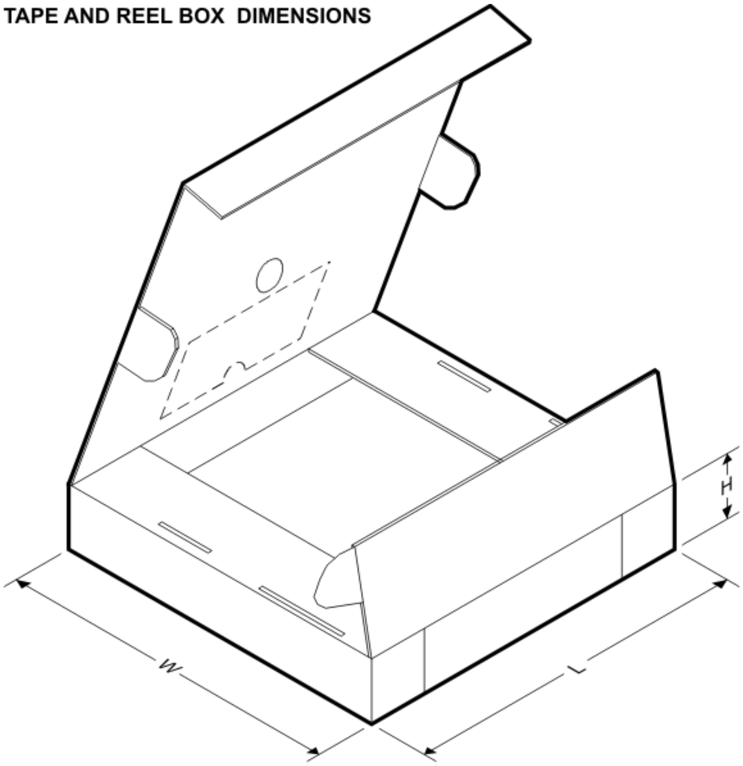
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP5010PMR	LQFP	PM	64	1000	330.0	25.4	12.8	12.8	1.9	16.0	24.0	Q2

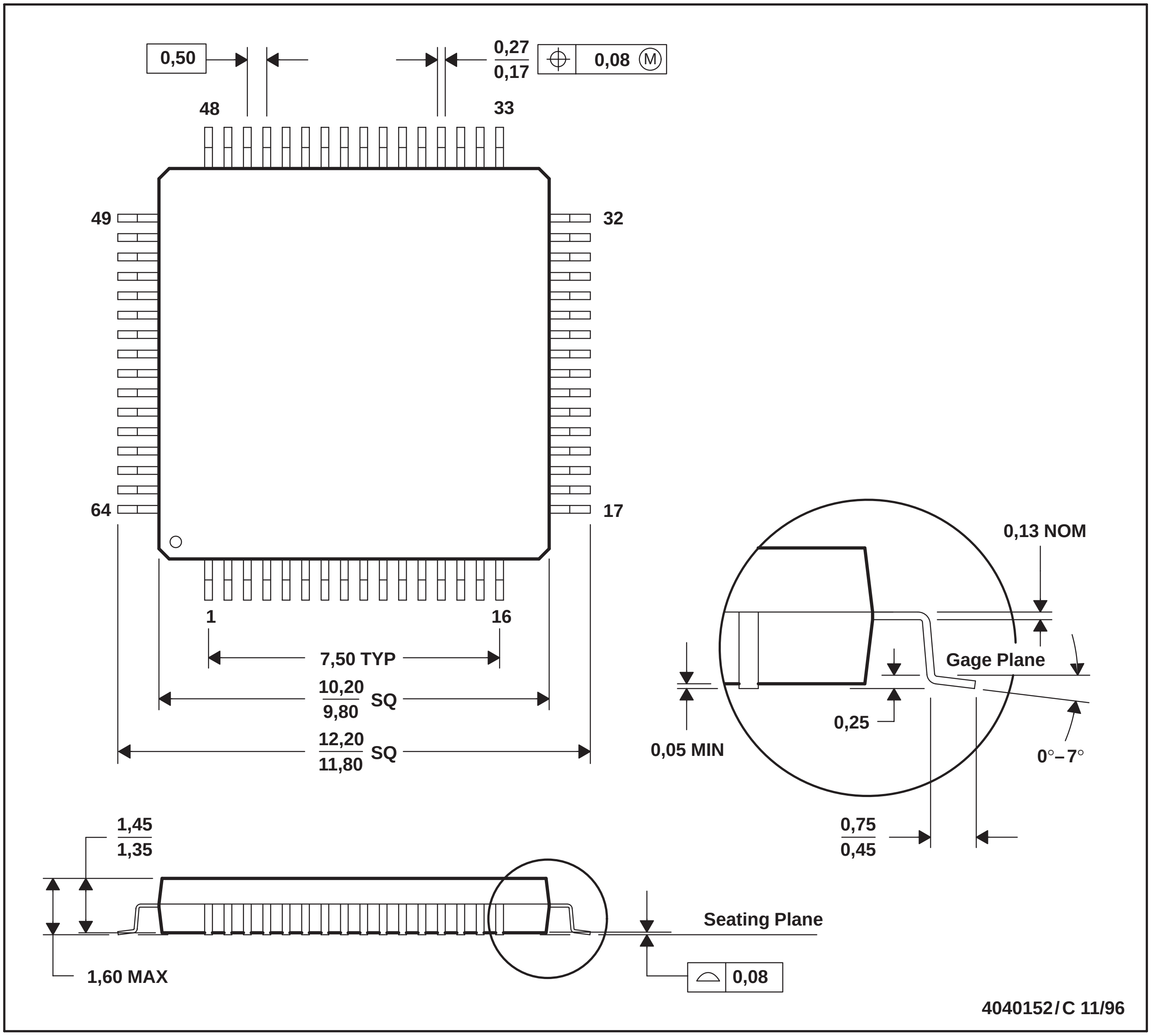
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

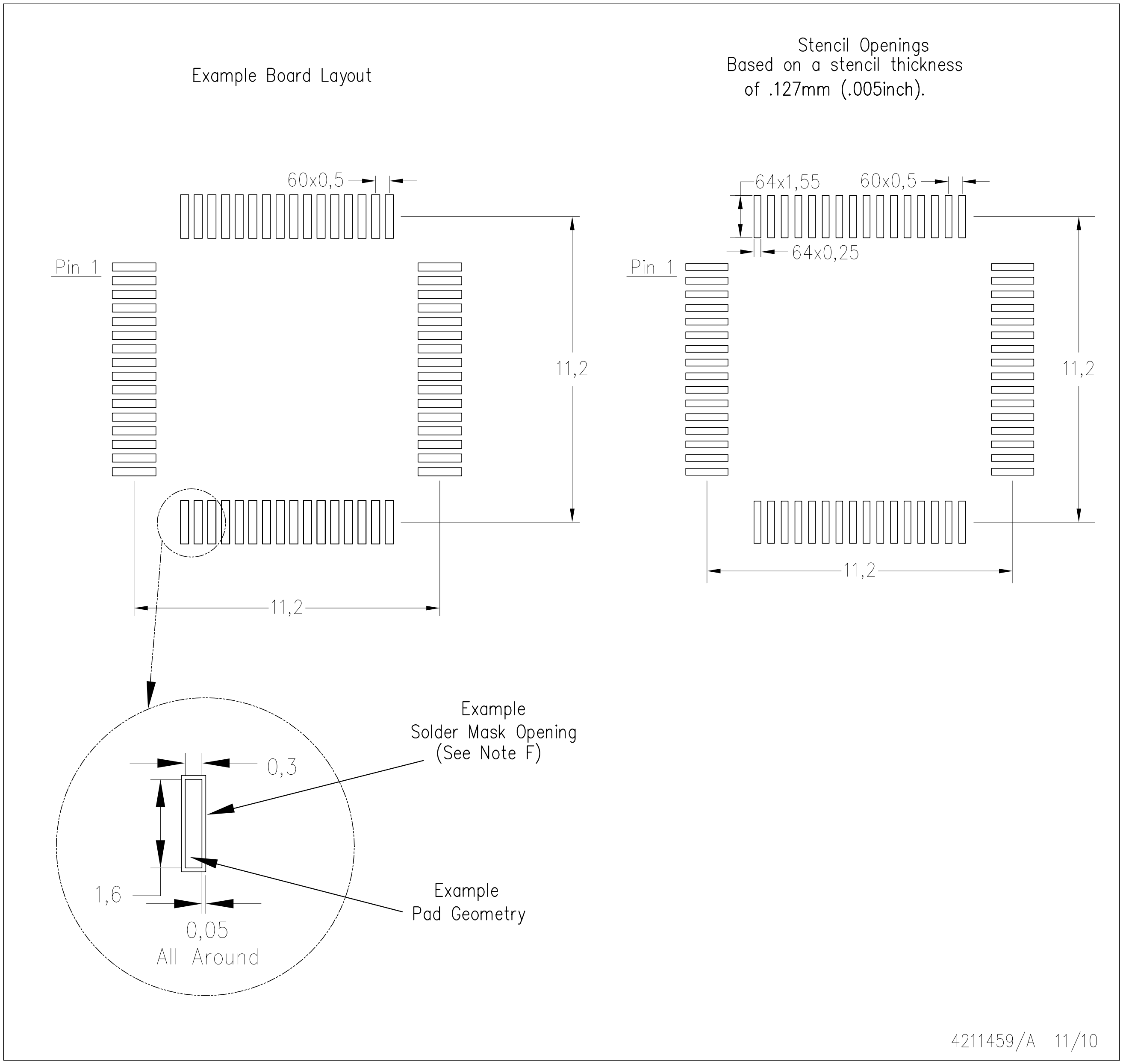
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP5010PMR	LQFP	PM	64	1000	367.0	367.0	45.0

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

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