

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

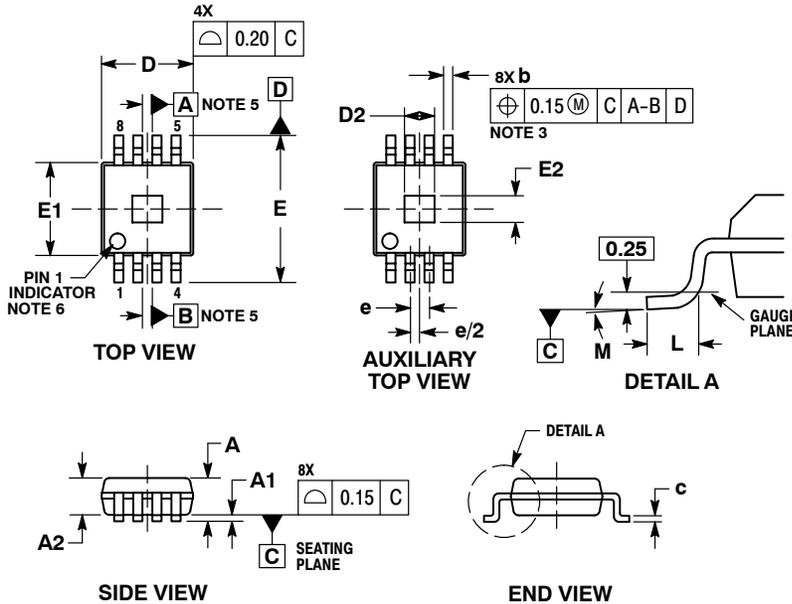


## CTSSOP8 3x3 CASE 949AA-01 ISSUE 0

DATE 17 JUL 2009



SCALE 2:1

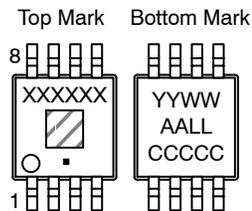


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION AND IS DETERMINED BETWEEN 0.08 AND 0.15 MM FROM THE LEAD TIP.
4. DIMENSIONS D AND E1 DOES NOT INCLUDE MOLD PROTRUSIONS, TIE BAR BURRS, GATE BURRS OR FLASH. END FLASH SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE ANY MOLD CAVITY MISMATCH AND ARE DETERMINED AT THE GAUGE PLANE.
5. DATUMS A AND B TO BE DETERMINED AT THE GAUGE PLANE.
6. DETAILS OF THE PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THIS ZONE.
7. D2 AND E2 DIMENSIONS FOR TOP SIDE OF PACKAGE DENOTE SENSOR WINDOW SIZE AND LOCATION.

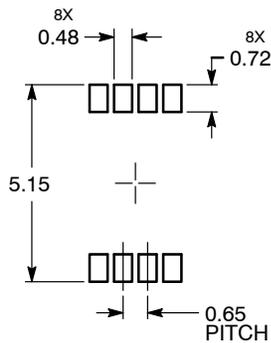
MILLIMETERS		
DIM	MIN	MAX
A	---	1.10
A1	0.00	0.14
A2	0.73	0.93
b	0.24	0.39
c	0.13	0.24
D	3.00 BSC	
D2	0.66	1.37
E	4.90 BSC	
E1	3.00 BSC	
E2	0.41	1.37
e	0.65 BSC	
L	0.39	0.67
M	0°	8°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- YY = Year
- WW = Work Week
- AA = Assembly Location
- LL = Wafer Lot
- CCCCC = Country of Origin
- = Pb-Free Package

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	CTSSOP8 3X3 WITH SENSOR WINDOW	PAGE 1 OF 2

