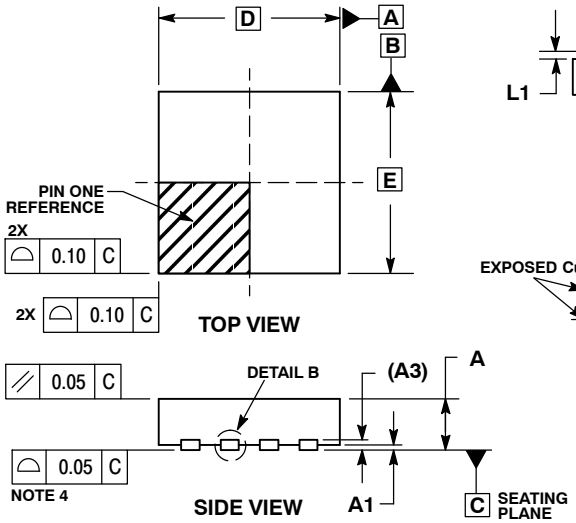
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

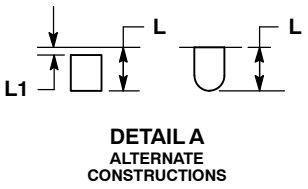
ON Semiconductor®

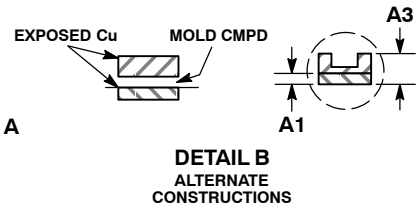
**DFN8, 3x3, 0.65P**
CASE 506BY
ISSUE A

DATE 23 MAY 2012

**SCALE 2:1**

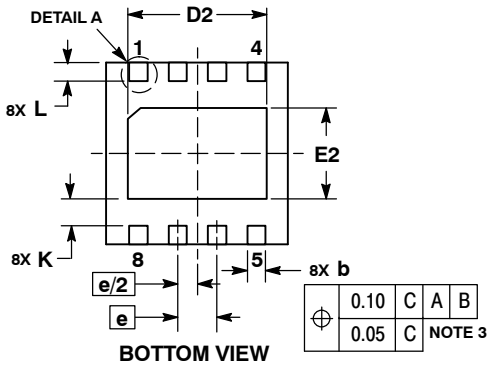



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL B ALTERNATE CONSTRUCTION IS NOT APPLICABLE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.25 | 0.35 |
| D | 3.00 BSC | |
| D2 | 2.20 | 2.40 |
| E | 3.00 BSC | |
| E2 | 1.40 | 1.60 |
| e | 0.65 BSC | |
| K | 0.20 | --- |
| L | 0.20 | 0.40 |
| L1 | 0.00 | 0.15 |



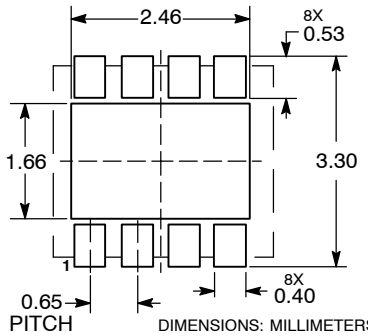

### GENERIC MARKING DIAGRAM*


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| STATUS: | ON SEMICONDUCTOR STANDARD | |
| NEW STANDARD: | | |
| DESCRIPTION: | DFN8, 3X3, 0.65P | PAGE 1 OF 2 |

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION. REQ. BY B. FONTES. | 23 MAR 2011 |
| A | ADDED NOTE 5. REQ. BY B. MARQUIS. | 23 MAY 2012 |
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