

MECHANICAL CASE OUTLINE

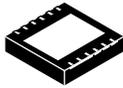
PACKAGE DIMENSIONS

ON Semiconductor®

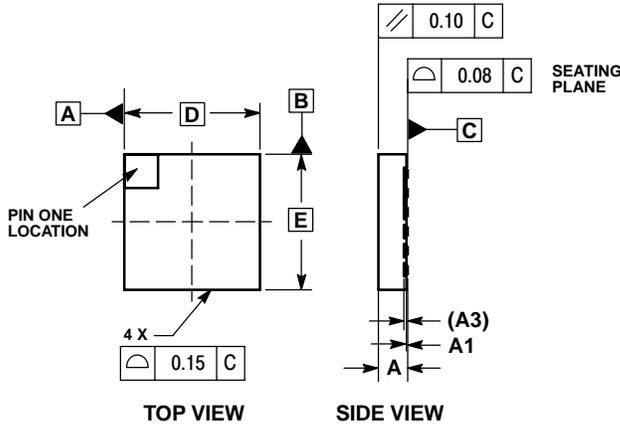


PLL-12, 9x9 mm
CASE 488AB-01
ISSUE C

DATE 18 JUL 2005



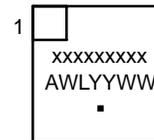
SCALE 1:1



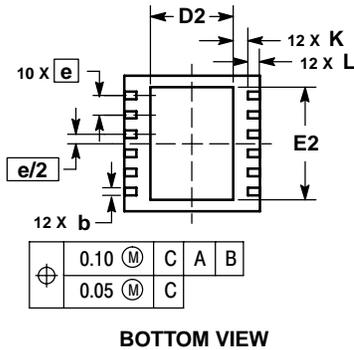
- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. DIMENSIONS IN MILLIMETERS.
 3. COPLANARITY APPLIES TO THE LEAD, DIMENSION B, AND EXPOSED PAD.

MILLIMETERS		
DIM	MIN	MAX
A	1.750	1.950
A1	0.000	0.050
A3	0.254 REF	
b	0.400	0.600
D	9.000 BSC	
E	9.000 BSC	
e	1.270 BSC	
D2	5.400	5.600
E2	7.400	7.600
K	0.850 REF	
L	0.850	0.950

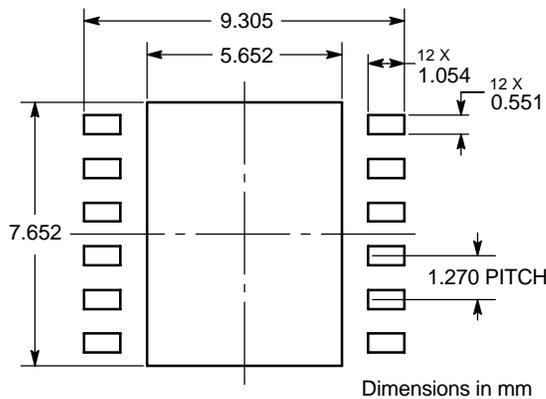
GENERIC MARKING DIAGRAM*



- xxxxxxx = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G or ■ = Pb-Free Package



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

- STYLE 1:
1. OVLO
 2. UVLO
 3. ENABLE/TIMER
 4. GND
 5. CCHARGE
 6. CURRENT LIMIT
 7. POWER GOOD
 8. N/C
 9. N/C
 10. SOURCE
 11. SOURCE
 12. SOURCE

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	PLL-12, 9*9 MM, SMART HOTPLUG	PAGE 1 OF 2

