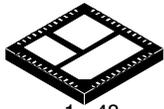


MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

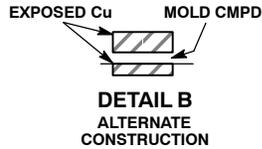
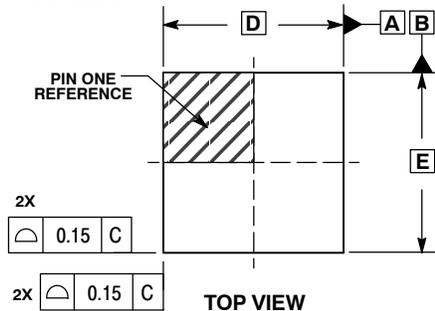


1 48

SCALE 2:1

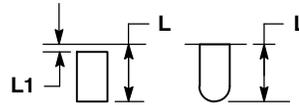
QFN48 6x6, 0.4P
CASE 485CJ
ISSUE A

DATE 09 AUG 2012

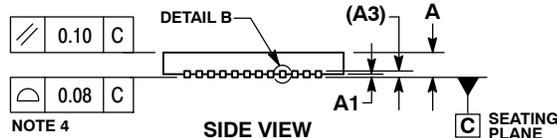


NOTES:

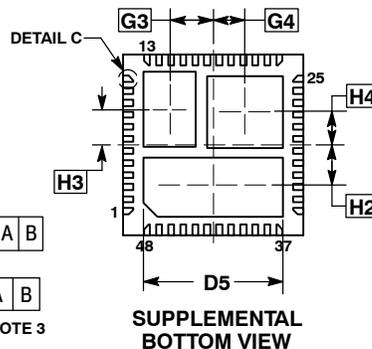
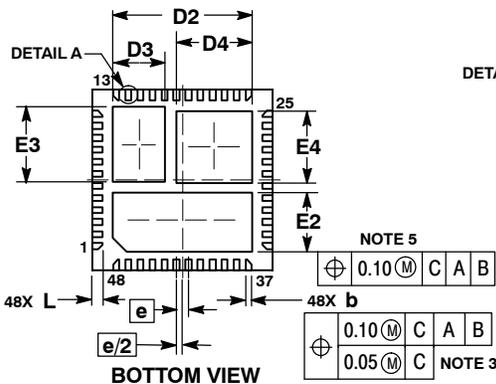
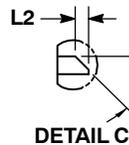
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS IN BOTH X AND Y AXIS.



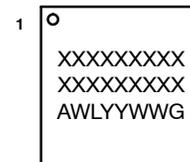
MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.15	0.25
D	6.00	BSC
D2	4.53	4.73
D3	1.64	1.84
D4	2.42	2.62
D5	4.58	4.78
E	6.00	BSC
E2	1.86	2.06
E3	2.41	2.61
E4	2.30	2.50
e	0.40	BSC
G3	1.45	BSC
G4	1.06	BSC
H2	1.40	BSC
H3	1.19	BSC
H4	1.10	BSC
L	0.25	0.45
L1	---	0.15
L2	0.15	REF



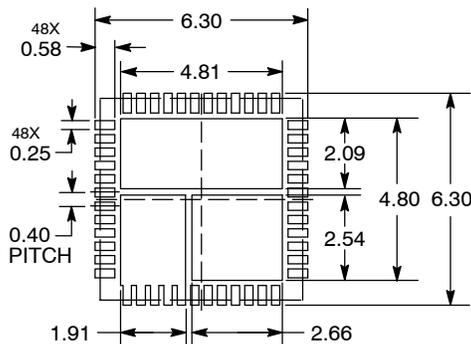
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



GENERIC
MARKING DIAGRAM*



RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

DOCUMENT NUMBER:	98AON80730E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	QFN48, 6x6, 0.4MM PITCH	PAGE 1 OF 2

