

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

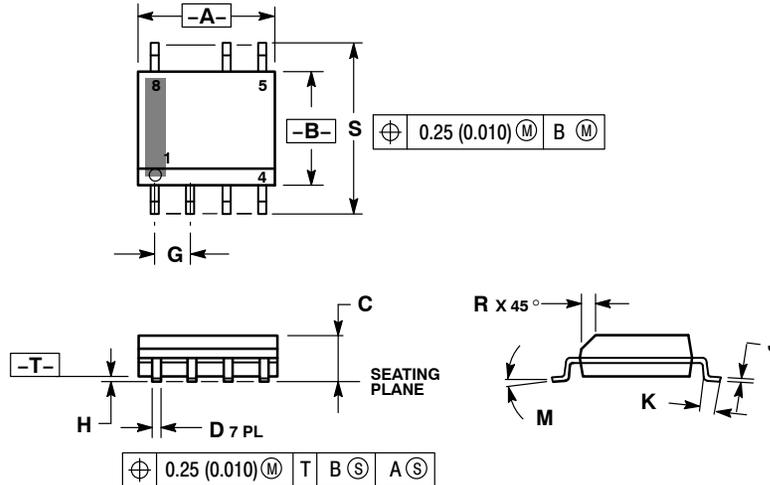
ON Semiconductor®



SCALE 1:1

SOIC-7
CASE 751U-01
ISSUE E

DATE 20 OCT 2009

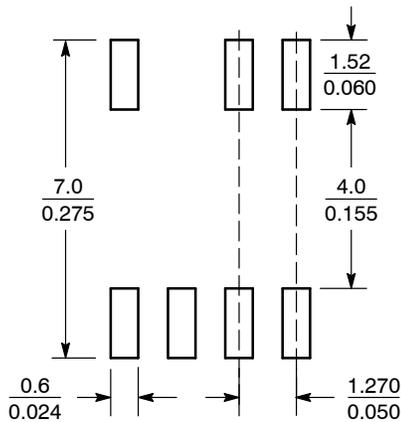


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

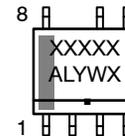
SOLDERING FOOTPRINT*



SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



- XXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLES ON PAGE 2

| | | |
|------------------|---------------------------|--|
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| STATUS: | ON SEMICONDUCTOR STANDARD | |
| NEW STANDARD: | | |
| DESCRIPTION: | 7-LEAD SOIC | PAGE 1 OF 3 |

SOIC-7
CASE 751U-01
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DATE 20 OCT 2009

STYLE 1:

- PIN 1. EMITTER
- 2. COLLECTOR
- 3. COLLECTOR
- 4. EMITTER
- 5. EMITTER
- 6.
- 7. NOT USED
- 8. EMITTER

STYLE 2:

- PIN 1. COLLECTOR, DIE, #1
- 2. COLLECTOR, #1
- 3. COLLECTOR, #2
- 4. COLLECTOR, #2
- 5. BASE, #2
- 6. EMITTER, #2
- 7. NOT USED
- 8. EMITTER, #1

STYLE 3:

- PIN 1. DRAIN, DIE #1
- 2. DRAIN, #1
- 3. DRAIN, #2
- 4. DRAIN, #2
- 5. GATE, #2
- 6. SOURCE, #2
- 7. NOT USED
- 8. SOURCE, #1

STYLE 4:

- PIN 1. ANODE
- 2. ANODE
- 3. ANODE
- 4. ANODE
- 5. ANODE
- 6. ANODE
- 7. NOT USED
- 8. COMMON CATHODE

STYLE 5:

- PIN 1. DRAIN
- 2. DRAIN
- 3. DRAIN
- 4. DRAIN
- 5.
- 6.
- 7. NOT USED
- 8. SOURCE

STYLE 6:

- PIN 1. SOURCE
- 2. DRAIN
- 3. DRAIN
- 4. SOURCE
- 5. SOURCE
- 6.
- 7. NOT USED
- 8. SOURCE

STYLE 7:

- PIN 1. INPUT
- 2. EXTERNAL BYPASS
- 3. THIRD STAGE SOURCE
- 4. GROUND
- 5. DRAIN
- 6. GATE 3
- 7. NOT USED
- 8. FIRST STAGE Vd

STYLE 8:

- PIN 1. COLLECTOR (DIE 1)
- 2. BASE (DIE 1)
- 3. BASE (DIE 2)
- 4. COLLECTOR (DIE 2)
- 5. COLLECTOR (DIE 2)
- 6. EMITTER (DIE 2)
- 7. NOT USED
- 8. COLLECTOR (DIE 1)

STYLE 9:

- PIN 1. EMITTER (COMMON)
- 2. COLLECTOR (DIE 1)
- 3. COLLECTOR (DIE 2)
- 4. EMITTER (COMMON)
- 5. EMITTER (COMMON)
- 6. BASE (DIE 2)
- 7. NOT USED
- 8. EMITTER (COMMON)

STYLE 10:

- PIN 1. GROUND
- 2. BIAS 1
- 3. OUTPUT
- 4. GROUND
- 5. GROUND
- 6. BIAS 2
- 7. NOT USED
- 8. GROUND

STYLE 11:

- PIN 1. SOURCE (DIE 1)
- 2. GATE (DIE 1)
- 3. SOURCE (DIE 2)
- 4. GATE (DIE 2)
- 5. DRAIN (DIE 2)
- 6. DRAIN (DIE 2)
- 7. NOT USED
- 8. DRAIN (DIE 1)

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