

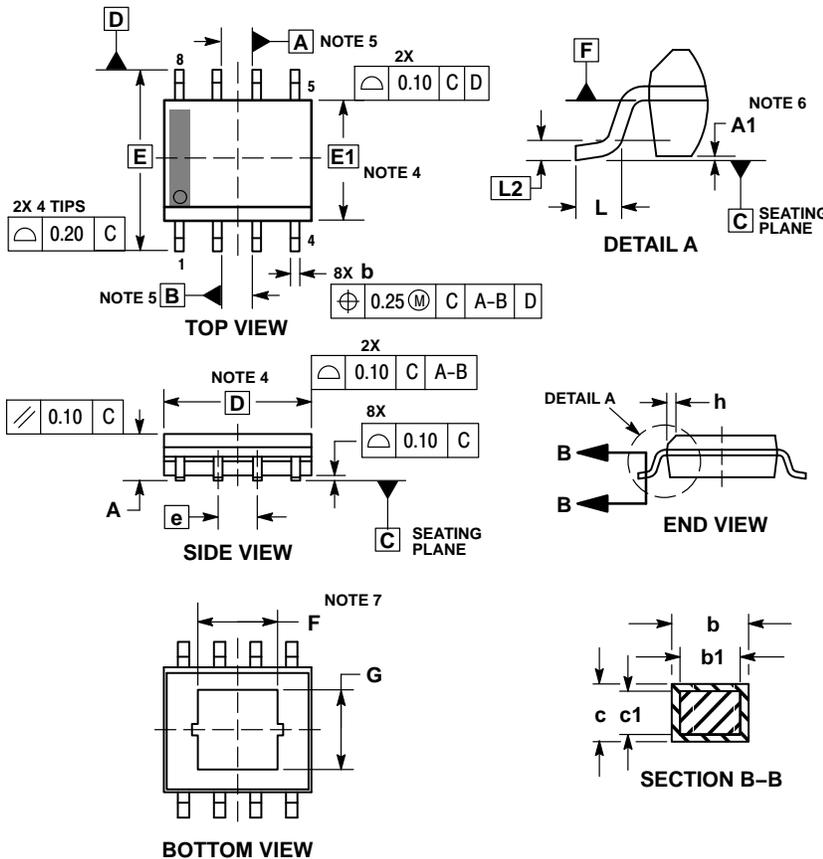
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SOIC8-NB EP CASE 751BU ISSUE E

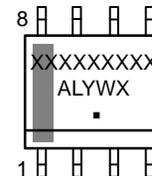
DATE 01 APR 2015



- NOTES:
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 - CONTROLLING DIMENSION: MILLIMETERS.
 - DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
 - DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
 - DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
 - A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
 - TAB CONTOUR MAY VARY MINIMALLY TO INCLUDE TOOLING FEATURES.

MILLIMETERS		
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
F	1.55	2.39
G	1.55	2.39
h	0.25	0.50
L	0.40	1.27
L2	0.25 BSC	

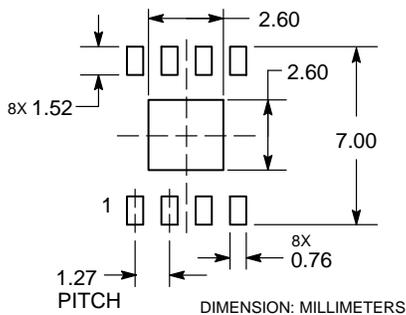
GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NEW STANDARD:		
DESCRIPTION:	SOIC8-NB EP	PAGE 1 OF 2

