

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

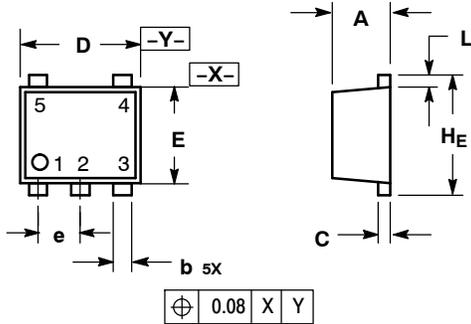
ON Semiconductor®



SOT-953
CASE 527AB-01
ISSUE C

DATE 30 JUL 2008

SCALE 4:1

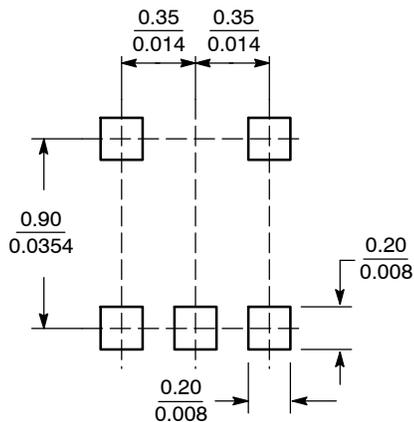


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.42	0.50	0.013	0.017	0.020
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.05	0.10	0.15	0.002	0.004	0.006
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
He	0.95	1.00	1.05	0.037	0.039	0.041

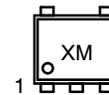
SOLDERING FOOTPRINT*



SCALE 20:1 ($\frac{\text{mm}}{\text{inches}}$)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- X = Specific Device Code
- M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	SOT-953, 1X1, 0.35P	PAGE 1 OF 1

