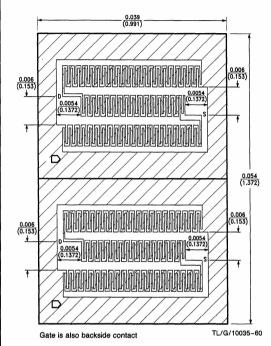


Process 59 N-Channel JFET



DESCRIPTION

Process 59 is provided for analog or digital switching applications where very low $R_{DS(ON)}$ is mandatory. The 4Ω typical ON resistance is very useful where switch resistance must be held to an absolute minimum.

Electrical Characteristics (T_A = 25°C)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
BV _{GSS}	Gate-Source Breakdown Voltage	$V_{DS} = 0V, I_{G} = -1 \mu A$	25			٧
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 15V$, $V_{GS} = 0V$ Pulse Test	100	600	1500	mA
I _{GSS}	Reverse Gate Leakage	$V_{GS} = -15V, V_{DS} = 0V$			1.0	nA
r _{DS(ON)}	ON Resistance	$V_{DS} = 100 \text{ mV}, V_{GS} = 0 \text{V}$	1.5	4.0	10	Ω
V _{GS(OFF)}	Pinch Off Voltage	V _{DS} = 5V, I _D = 100 nA	0.5	5.0	10	٧
I _{D(OFF)}	Drain OFF Current	$V_{DS} = 5V, V_{GS} = -10V$		1.0	10	nA
C _{rss}	Feedback Capacitance	$V_{DG} = 15V, I_{D} = 2 \text{ mA}, f = 1 \text{ MHz}$		25	35	pF
C _{iss}	Input Capacitance	$V_{DG} = 15V, I_{D} = 2 \text{ mA}, f = 1 \text{ MHz}$		50	80	pF
9fs	Forward Transconductance	$V_{DG} = 10V, I_{D} = 2 \text{ mA}$		10		mmho
9 _{os}	Output Conductance	$V_{DG} = 10V, I_{D} = 2 \text{ mA}$		200		μmho
en	Noise Voltage	$V_{DG} = 15V, I_D = 2 \text{ mA}, f = 100 \text{ Hz}$		6.0		nV/√Hz

This process is available in the following device types.

TO-92 (NS Package 92)

J105

J106

J107