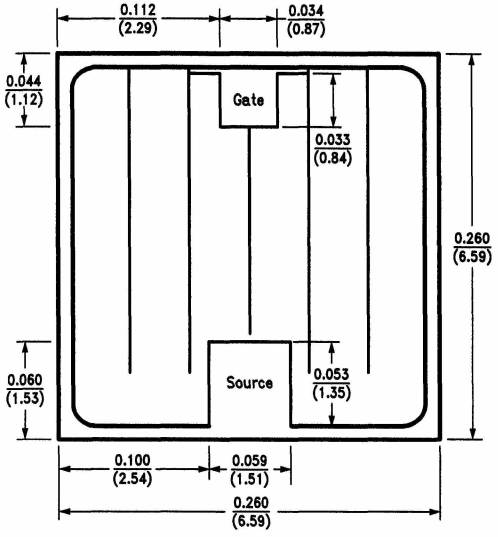
National Semiconductor

Process F2
N-Channel Power MOSFET



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DESCRIPTION

These dice are n-channel, enhancement mode, power MOSFETs designed especially for high power, high speed applications, such as power supplies, AC and DC motor control and high energy pulse circuits.

This process is available in the following device types:

TO-204 (Case 43)	TO-247 (Case 40)
IRF250CF	IRFP250CF
IRF250	IRFP250
IRF251	IRFP251
IRF252	IRFP252
IRF253	IRFP253

Electrical Characteristics T_C = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{DSS}	Drain to Source Voltage (Note 1)	I_D = 250 μA; V_{GS} = 0V	200		V
I_{DSS}	Zero Gate Voltage Drain	V_{DS} = Rated Voltage V_{GS} = 0V		250	μA
I_{GSS}	Gate Leakage Current	V_{DS} = ±20V; V_{DS} = 0V		±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	I_D = 250 μA; V_{DS} = V_{GS}	2.0	4.0	V
$R_{DS(ON)}$	Static On-Resistance (Note 2)	V_{GS} = 10V; I_D = 16A		0.085	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10V; I_D = 16A	8.0		Siemens
C_{iss}	Input Capacitance	V_{DS} = 25V; V_{GS} = 0V f = 1 MHz		3000	pF
C_{oss}	Output Capacitance			1200	pF
C_{rss}	Reverse Transfer			500	pF
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 95V; I_D = 16A V_{GS} = 10V; R_{GEN} = 4.7Ω		75	ns
t_r	Rise Time	R_{GS} = 4.7Ω		300	ns
$t_{d(off)}$	Turn-Off Delay Time			275	ns
t_f	Fall Time			150	ns
Q_g	Total Gate Charge	V_{GS} = 10V; I_D = 38A V_{DD} = 100V		120	nC

Note 1: T_J = +25°C to +150°C.

Note 2: Pulse Test: Pulse Width ≤ 80 μs, Duty Cycle ≤ 1%.

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Typical Performance Characteristics

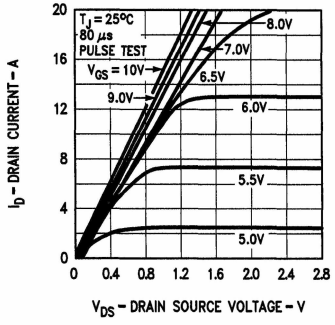

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FIGURE 1. Output Characteristics

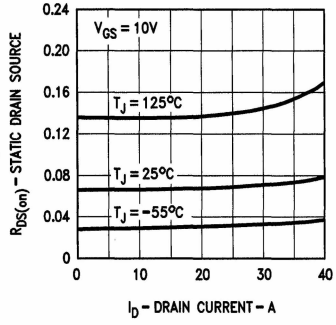

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FIGURE 2. Static Drain to Source Resistance vs Drain Current

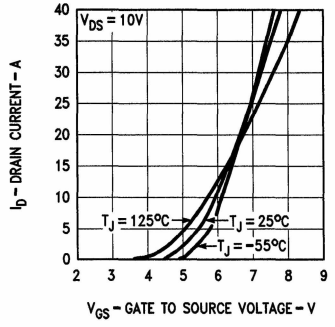

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FIGURE 3. Transfer Characteristics

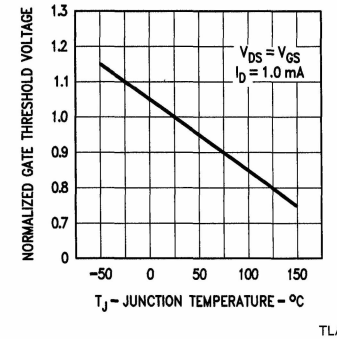

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FIGURE 4. Temperature Variation of Gate to Source Threshold Voltage

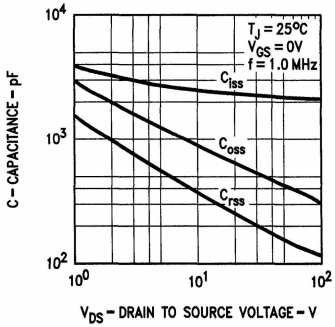

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FIGURE 5. Capacitance vs Drain to Source Voltage

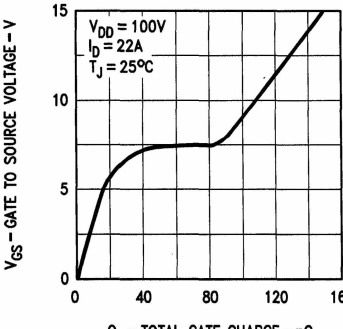

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FIGURE 6. Gate to Source Voltage vs Total Gate Charge

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Typical Performance Characteristics (Continued)

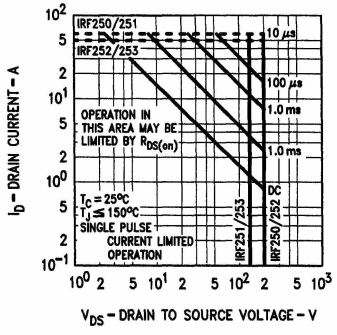

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FIGURE 7. Forward Biased Safe Operating Area

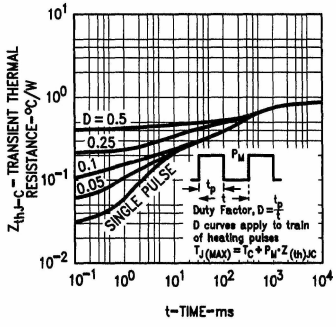

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FIGURE 8. Transient Thermal Resistance vs Time

Typical Electrical Characteristics

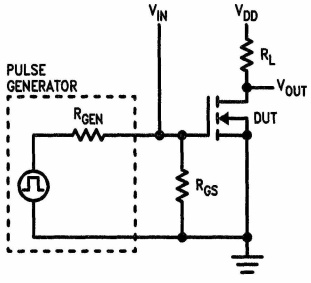

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FIGURE 9. Switching Test Circuit

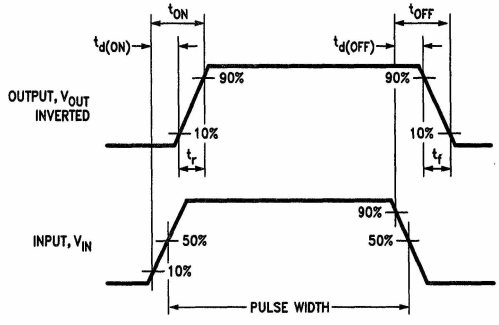

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FIGURE 10. Switching Waveforms

Probe Testing

Each die is probed and electrically tested to the limits specified in the Electrical Characteristics Table. However, high current parameters and thermal characteristics specified in the packaged device data sheets cannot be tested or guaranteed in die form because of the power dissipation limits of unmounted die and current handling limits of probe tips.

These parameters are:

Thermal Resistance
Forward Voltage Drop at Rated Current
Reverse Recovery Characteristics at Rated Current
Surge Current