

TL/G/10040-1

### DESCRIPTION

These dice are n-channel, enhancement mode, power MOSFETs designed especially for high power, high speed applications, such as power supplies, AC and DC motor control and high energy pulse circuits.

This process is available in the following device types:

TO-220 (Case 37)

IRF510

IRF511

IRF512

IRF513

MTP4N08

MTP4N10

### Electrical Characteristics $T_C = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{DS}$	Drain to Source Voltage (Note 1)	$I_D = 250 \mu\text{A}; V_{GS} = 0\text{V}$	100		V
$I_{DSS}$	Zero Gate Voltage Drain	$V_{DS} = \text{Rated Voltage}$ $V_{GS} = 0\text{V}$		250	$\mu\text{A}$
$I_{GSS}$	Gate Leakage Current	$V_{DS} = \pm 20\text{V}; V_{GS} = 0\text{V}$		100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$I_D = 250 \mu\text{A}; V_{DS} = V_{GS}$	2.0	4.0	V
$R_{DS(ON)}$	Static On-Resistance (Note 2)	$V_{GS} = 10\text{V}; I_D = 2.0\text{A}$		0.60	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}; I_D = 2.0\text{A}$	1.0		Siemens
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}; V_{GS} = 0\text{V}$ $f = 1 \text{ MHz}$		200	pF
$C_{oss}$	Output Capacitance			100	pF
$C_{rss}$	Reverse Transfer			30	pF
$t_{d(on)}$	Turn-On Delay Time (Note 3)	$V_{DD} = 50\text{V}; I_D = 2.0\text{A}$ $V_{GS} = 10\text{V}; R_{GEN} = 50\Omega$		20	ns
$t_r$	Rise Time	$R_{GS} = 50\Omega$		25	ns
$t_{d(off)}$	Turn-Off Delay Time			25	ns
$t_f$	Fall Time			20	ns
$Q_g$	Total Gate Charge	$V_{GS} = 10\text{V}; I_D = 8.0\text{A}$ $V_{DD} = 40\text{V}$		7.5	nC

**Note 1:**  $T_J = +25^\circ\text{C}$  to  $+150^\circ\text{C}$ .

**Note 2:** Pulse Test: Pulse Width  $\leq 80 \mu\text{s}$ , Duty Cycle  $\leq 1\%$ .

**Note 3:** Switching time measurements performed on LEM TR-58 test equipment.

# Process A1

## Typical Performance Characteristics

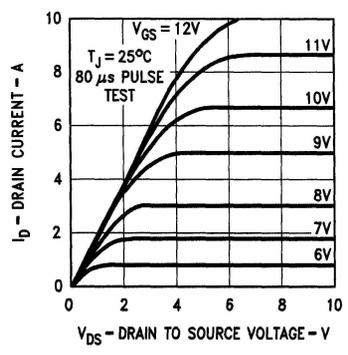


FIGURE 1. Output Characteristics TL/G/10040-2

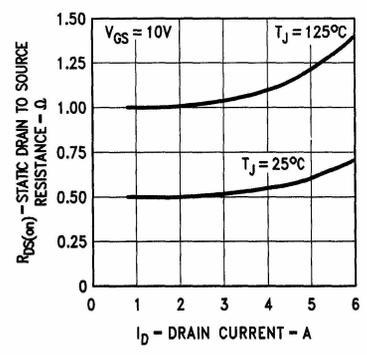


FIGURE 2. Static Drain to Source Resistance vs Drain Current TL/G/10040-3

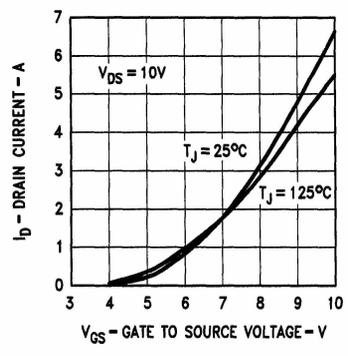


FIGURE 3. Transfer Characteristics TL/G/10040-4

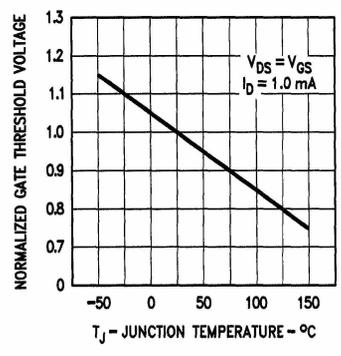


FIGURE 4. Temperature Variation of Gate to Source Threshold Voltage TL/G/10040-5

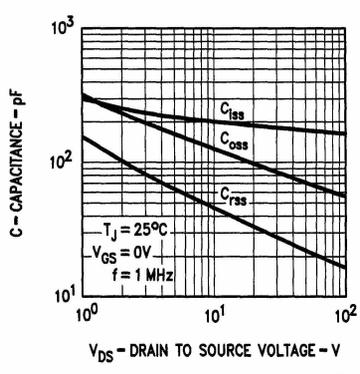


FIGURE 5. Capacitance vs Drain to Source Voltage TL/G/10040-6

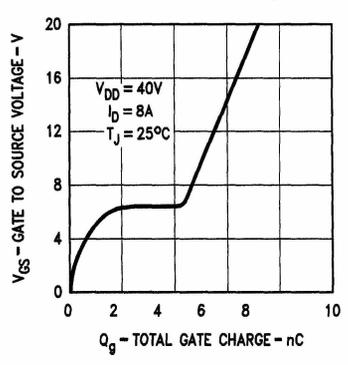


FIGURE 6. Gate to Source Voltage vs Total Gate Charge TL/G/10040-7

Typical Performance Characteristics (Continued)

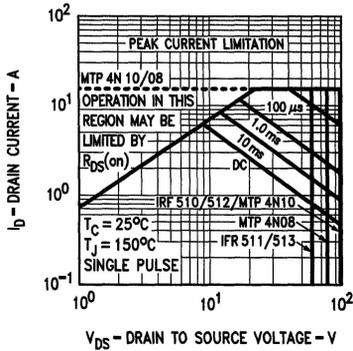


FIGURE 7. Forward Biased Safe Operating Area for MTP4N08/4N10

TL/G/10040-8

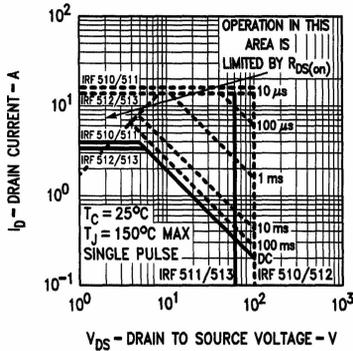


FIGURE 9. Forward Biased Safe Operating Area for IRF510-513

TL/G/10040-10

Typical Electrical Characteristics

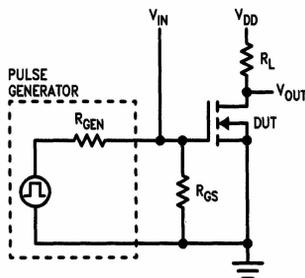


FIGURE 11. Switching Test Circuit

TL/G/10040-12

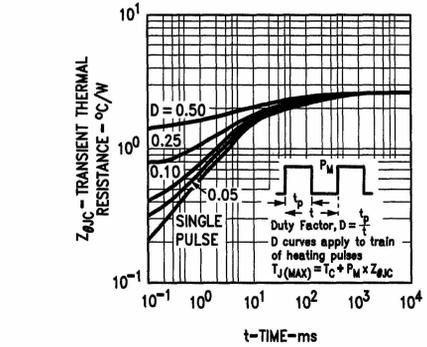


FIGURE 8. Transient Thermal Resistance vs Time for MTP4N08/4N10

TL/G/10040-9

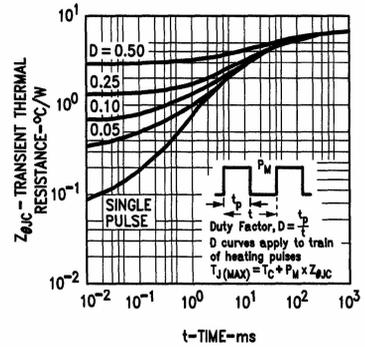


FIGURE 10. Transient Thermal Resistance vs Time for IRF510-513

TL/G/10040-11

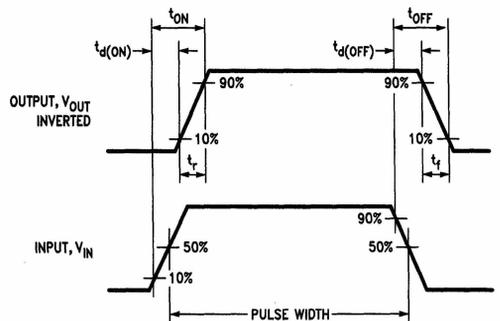


FIGURE 12. Switching Waveforms

TL/G/10040-13