Bulletin I25180 rev. A 04/94

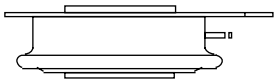
International
IOR Rectifier

ST173C..C SERIES

INVERTER GRADE THYRISTORS

Hockey Puk Version

330A



case style TO-200AB (A-PUK)

Features

- Metal case with ceramic insulator
- International standard case TO-200AB (A-PUK)
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- High surge current capability
- Low thermal impedance
- High speed performance

TypicalApplications

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

Major Ratings and Characteristics

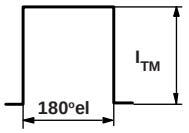
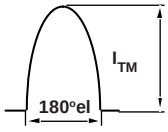
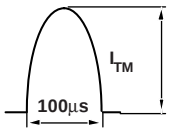
Parameters		ST173C..C	Units
$I_{T(AV)}$		330	A
	@ T_{hs}	55	°C
$I_{T(RMS)}$		610	A
	@ T_{hs}	25	°C
I_{TSM}	@ 50Hz	4680	A
	@ 60Hz	4900	A
I^2t	@ 50Hz	110	KA^2s
	@ 60Hz	100	KA^2s
V_{DRM}/V_{RRM}		1000 to1200	V
t_q range		15 to 30	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM}, maximum repetitive peak voltage V	V_{RSM}, maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J$ max. mA
ST173C..C	10	1000	1100	40
	12	1200	1300	

Current Carrying Capability

Frequency							Units
50Hz	760	660	1200	1030	5570	4920	A
400Hz	730	590	1260	1080	2800	2460	
1000Hz	600	490	1200	1030	1620	1390	
2500Hz	350	270	850	720	800	680	
Recovery voltage Vr	50	50	50	50	50	50	V
Voltage before turn-on Vd	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50	50	-	-	-	-	A/µs
Heatsink temperature	40	55	40	55	40	55	°C
Equivalent values for RC circuit	47Ω / 0.22µF		47Ω / 0.22µF		47Ω / 0.22µF		

On-state Conduction

	Parameter	ST173C..C	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current	330 (120)	A	180° conduction, half sine wave		
	@ Heatsink temperature	55 (85)	°C	double side (single side) cooled		
$I_{T(RMS)}$	Max. RMS on-state current	610	A	DC @ 25°C heatsink temperature double side cooled		
I_{TSM}	Max. peak, one half cycle, non-repetitive surge current	4680	A	t = 10ms	No voltage reapplied	Sinusoidal half wave, Initial $T_J = T_J$ max
		4900		t = 8.3ms		
		3940		t = 10ms	100% V_{RRM} reapplied	
		4120		t = 8.3ms		
I^2t	Maximum I^2t for fusing	110	KA^2s	t = 10ms	No voltage reapplied	
		100		t = 8.3ms		
		77		t = 10ms	100% V_{RRM} reapplied	
		71		t = 8.3ms		
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	1100	$KA^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied		

On-state Conduction

	Parameter	ST173C..C	Units	Conditions
V_{TM}	Max. peak on-state voltage	2.07	V	I_{TM}= 600A, T_J = T_J max, t_p = 10ms sine wave pulse
$V_{T(TO)1}$	Low level value of threshold voltage	1.55		(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = T_J max.
$V_{T(TO)2}$	High level value of threshold voltage	1.61		(I > π x $I_{T(AV)}$), T_J = T_J max.
r_{t1}	Low level value of forward slope resistance	0.87	mΩ	(16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = T_J max.
r_{t2}	High level value of forward slope resistance	0.77		(I > π x $I_{T(AV)}$), T_J = T_J max.
I_H	Maximum holding current	600	mA	T_J = 25°C, I_T > 30A
I_L	Typical latching current	1000		T_J = 25°C, V_A= 12V, Ra = 6Ω, I_G= 1A

Switching

	Parameter	ST173C..C		Units	Conditions
di/dt	Max. non-repetitive rate of rise of turned-on current	1000		A/µs	T_J = T_J max, V_{DRM} = rated V_{DRM} I_{TM} = 2 x di/dt
t_d	Typical delay time	1.1		µs	T_J= 25°C, V_{DM} = rated V_{DRM}, I_{TM} = 50A DC, t_p= 1µs Resistive load, Gate pulse: 10V, 5Ω source
		Min	Max		
t_q	Max. turn-off time	15	30		T_J = T_J max, I_{TM} = 300A, commutating di/dt = 20A/µs V_R = 50V, t_p = 500µs, dv/dt: see table in device code

Blocking

	Parameter	ST173C..C	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	500	V/µs	T_J = T_J max. linear to 80% V_{DRM}, higher value available on request
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current	40	mA	T_J = T_J max, rated V_{DRM}/V_{RRM} applied

Triggering

	Parameter	ST173C..C	Units	Conditions
P_{GM}	Maximum peak gate power	60	W	T_J = T_J max, f = 50Hz, d% = 50
$P_{G(AV)}$	Maximum average gate power	10		
I_{GM}	Max. peak positive gate current	10	A	T_J = T_J max, t_p ≤ 5ms
$+V_{GM}$	Maximum peak positive gate voltage	20	V	T_J = T_J max, t_p ≤ 5ms
$-V_{GM}$	Maximum peak negative gate voltage	5		
I_{GT}	Max. DC gate current required to trigger	200	mA	T_J = 25°C, V_A = 12V, Ra = 6Ω
V_{GT}	Max. DC gate voltage required to trigger	3	V	
I_{GD}	Max. DC gate current not to trigger	20	mA	T_J = T_J max, rated V_{DRM} applied
V_{GD}	Max. DC gate voltage not to trigger	0.25	V	

Thermal and Mechanical Specification

	Parameter	ST173C..C	Units	Conditions
T_J	Max. operating temperature range	-40 to 125	°C	
T_{stg}	Max. storage temperature range	-40 to 150		
R_{thJ-hs}	Max. thermal resistance, junction to heatsink	0.17 0.08	K/W	DC operation single side cooled DC operation double side cooled
R_{thC-hs}	Max. thermal resistance, case to heatsink	0.033 0.017	K/W	DC operation single side cooled DC operation double side cooled
F	Mounting force, ± 10%	4900 (500)	N (Kg)	
wt	Approximate weight	50	g	
	Case style	TO - 200AB (A-PUK)		See Outline Table

ΔR_{thJ-hs} Conduction

(The following table shows the increment of thermal resistence R_{thJ-hs} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction		Rectangular conduction		Units	Conditions
	Single Side	Double Side	Single Side	Double Side		
180°	0.015	0.016	0.011	0.011	K/W	$T_J = T_J$ max.
120°	0.018	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.037		
30°	0.060	0.060	0.060	0.061		

Ordering Information Table

Device Code

ST	17	3	C	12	C	H	K	1	
1	2	3	4	5	6	7	8	9	10

1 - Thyristor

2 - Essential part number

3 - 3 = Fast turn off

4 - C = Ceramic Puk

5 - Voltage code: Code x 100 = V_{RRM} (See Voltage Rating Table)

6 - C = Puk Case TO-200AB (A-PUK)

7 - Reapplied dv/dt code (for t_q test condition)

8 - t_q code

9 - 0 = Eyelet term. (Gate and Aux. Cathode Unsoldered Leads)
1 = Fast-on term. (Gate and Aux. Cathode Unsoldered Leads)
2 = Eyelet term. (Gate and Aux. Cathode Soldered Leads)
3 = Fast-on term. (Gate and Aux. Cathode Soldered Leads)

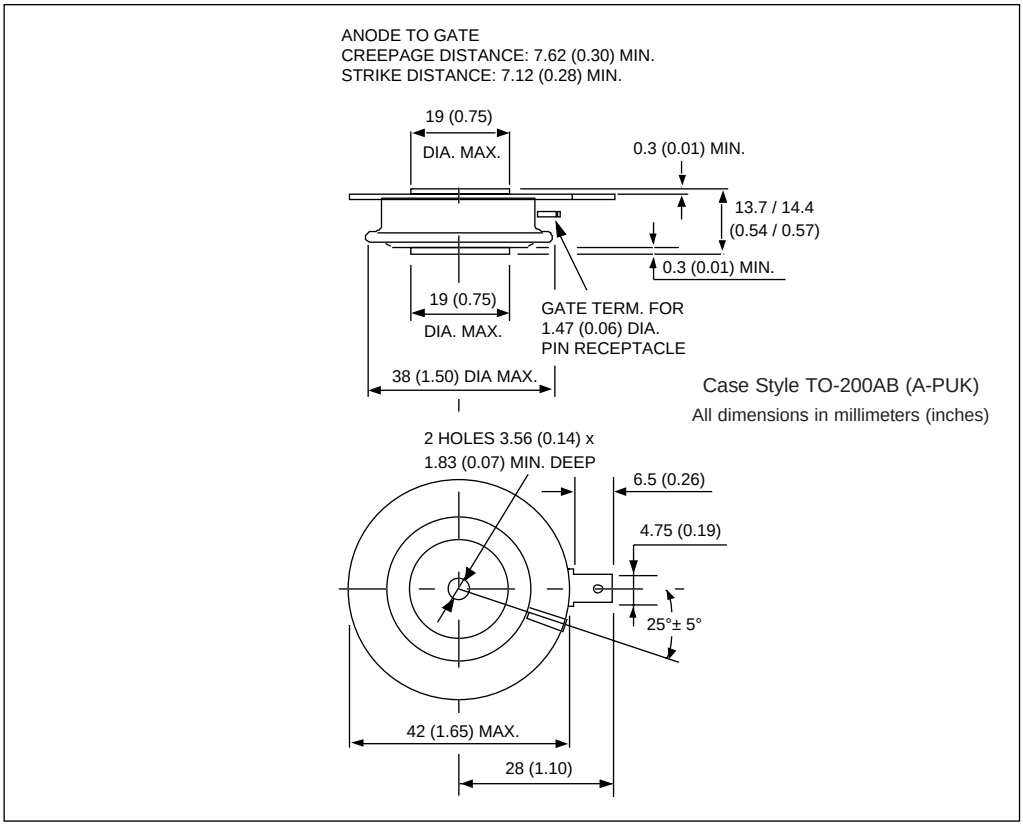
10 - Critical dv/dt:
None = 500V/µsec (Standard value)
L = 1000V/µsec (Special selection)

dv/dt - t_q combinations available

dv/dt (V/µs)	20	50	100	**200**	400
t_q(µs) 15	CL	--	--	--	--
t_q(µs) 18	CP	DP	EP	**FP ***	--
t_q(µs) 20	CK	DK	EK	**FK ***	HK
t_q(µs) 25	CJ	DJ	EJ	FJ	HJ
t_q(µs) 30	--	DH	EH	FH	HH

*****Standard part number.
All other types available only on request.

Outline Table



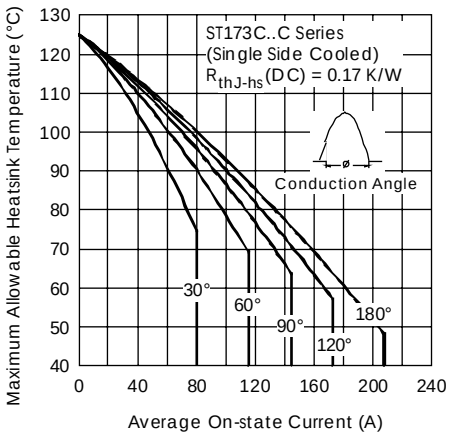


Fig. 1 - Current Ratings Characteristics

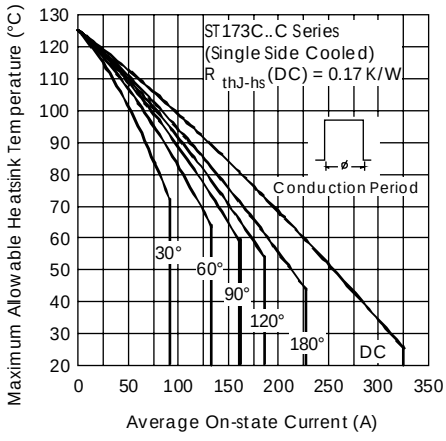


Fig. 2 - Current Ratings Characteristics

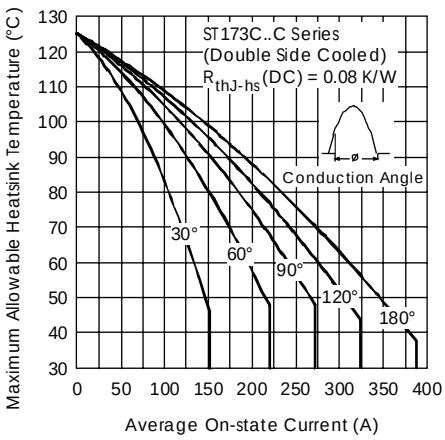


Fig. 3 - Current Ratings Characteristics

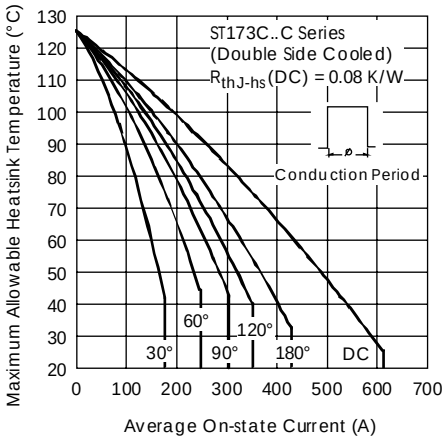


Fig. 4 - Current Ratings Characteristics

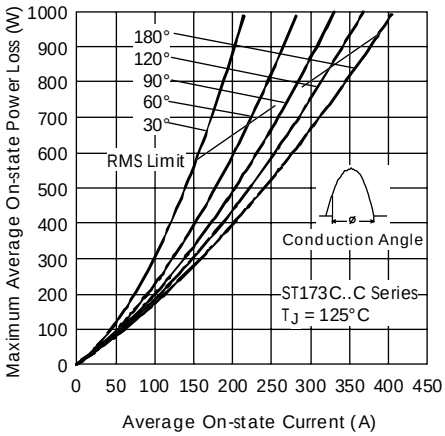


Fig. 5 - On-state Power Loss Characteristics

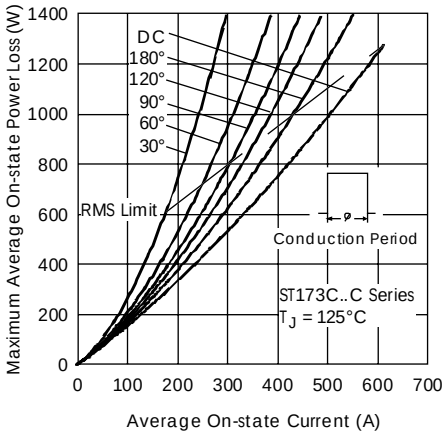


Fig. 6 - On-state Power Loss Characteristics

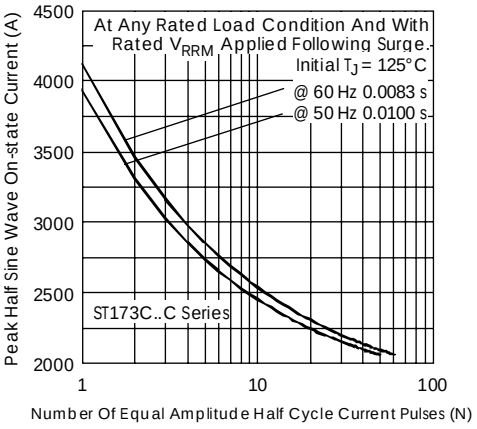


Fig. 7 - Maximum Non-repetitive Surge Current
Single and Double Side Cooled

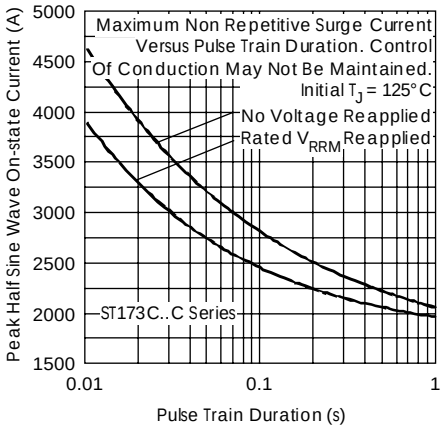


Fig. 8 - Maximum Non-repetitive Surge Current
Single and Double Side Cooled

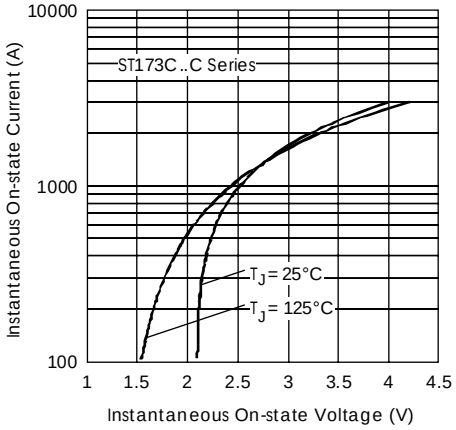


Fig. 9 - On-state Voltage Drop Characteristics

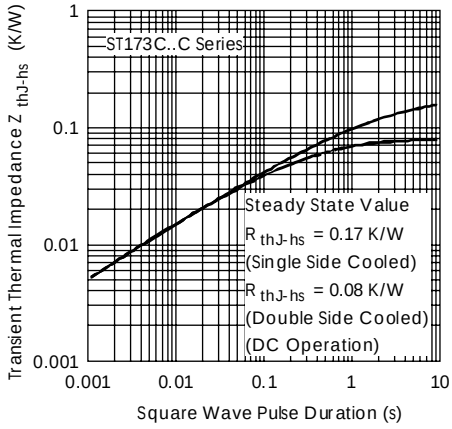


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

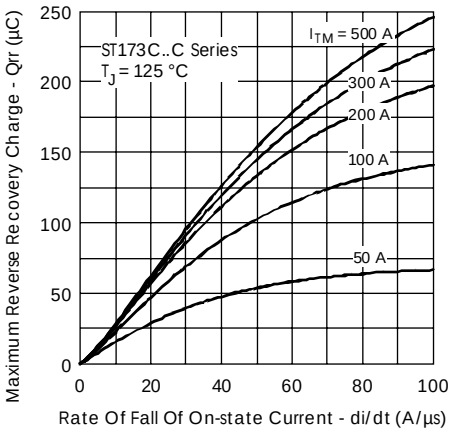


Fig. 11 - Reverse Recovered Charge Characteristics

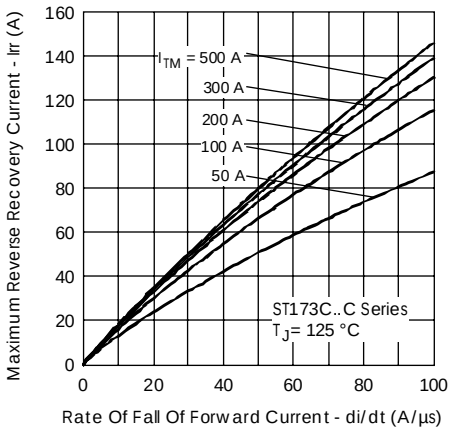


Fig. 12 - Reverse Recovery Current Characteristics

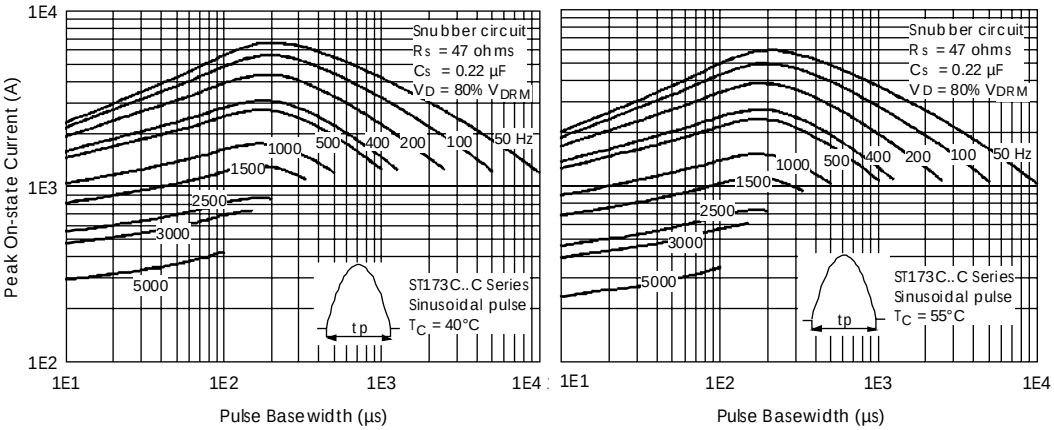


Fig. 13 - Frequency Characteristics

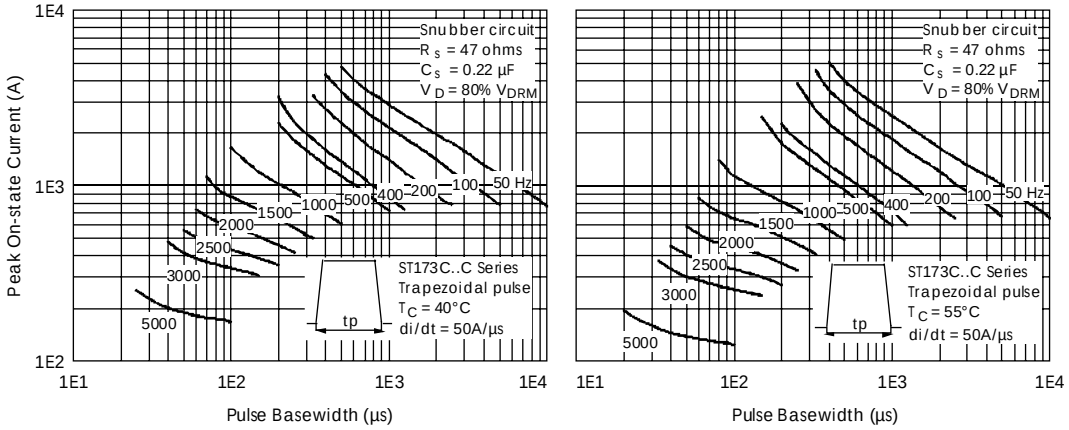


Fig. 14 - Frequency Characteristics

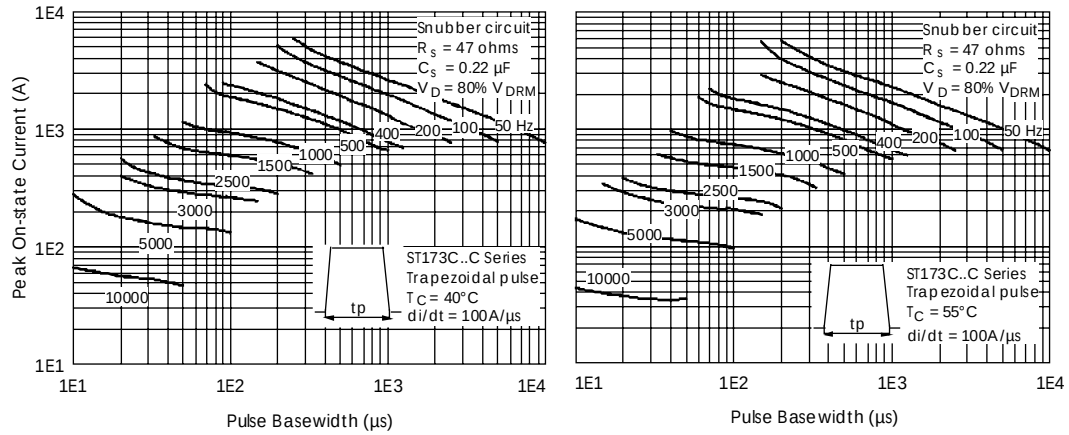


Fig. 15 - Frequency Characteristics

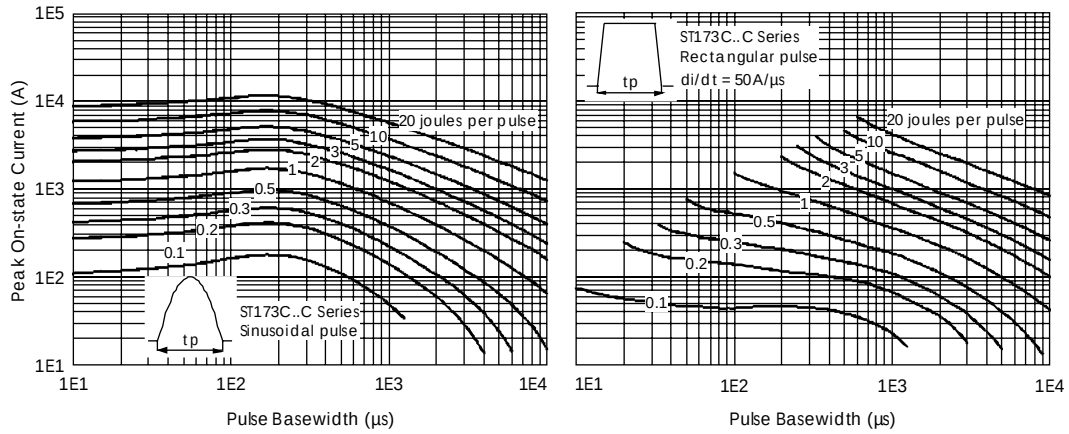


Fig. 16 - Maximum On-state Energy Power Loss Characteristics

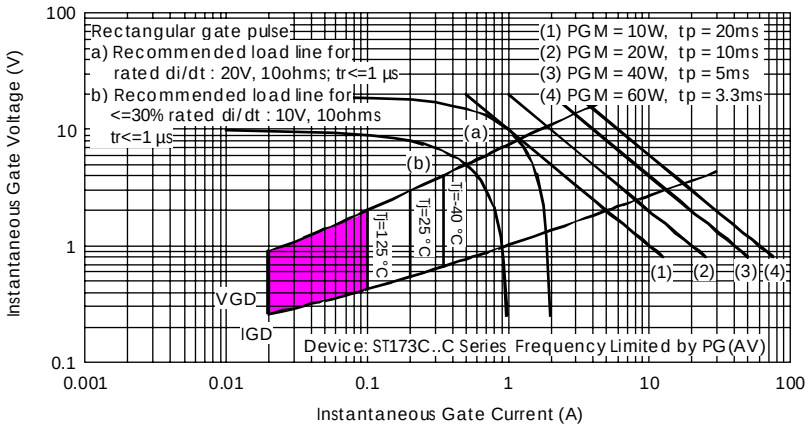


Fig. 17 - Gate Characteristics