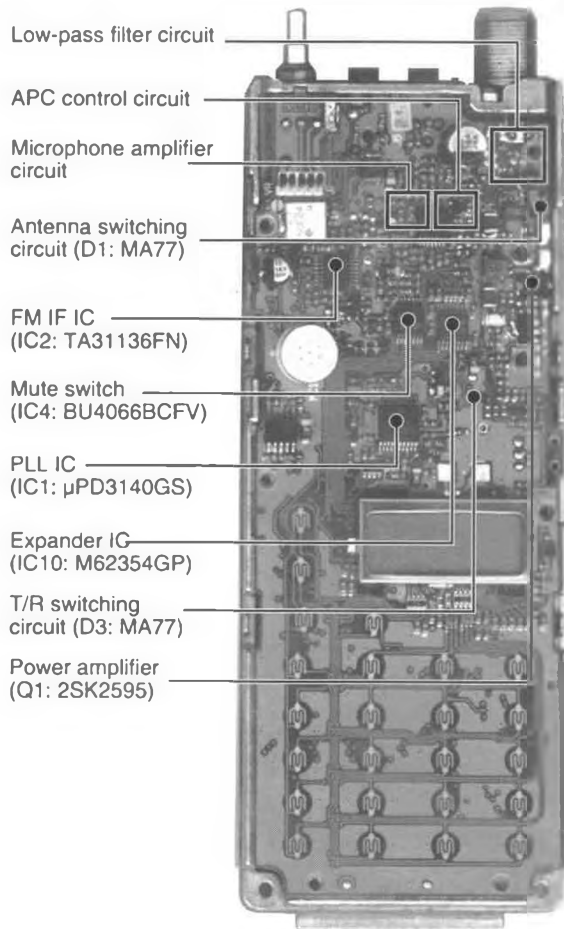


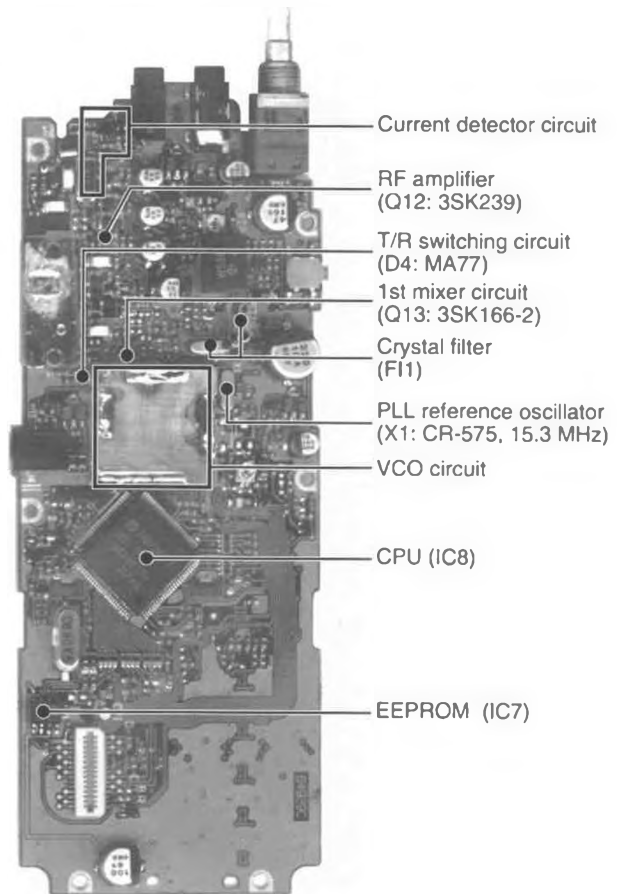
			IC-F3, IC-F3S		IC-F4, IC-F4S	
GENERAL	Frequency coverage		136.000–150.000 MHz (L-band) 146.000–174.000 MHz (H-band)		400.000–430.000 MHz (L-band) 440.000–470.000 MHz (H-band)	
	Mode		16K0F3E (W-type), 14K0F3E (M-type; IC-F3/S only), 8K50F3E (N-type)			
	Number of channels		32 (16 channels × 2 banks: 2-BANK version), 16 (16 channel version)			
	Power supply requirement		9.6 V DC (negative ground: supplied battery pack)			
	Current drain	Tx	at high	1.3 A	1.4 A	
			at low	0.6 A	0.7 A	
		Rx	rated audio	250 mA	250 mA	
			stand-by	60 mA typ.	60mA typ.	
	Frequency stability		±0.0005 % (EIA), ±2,000 Hz (ETS/CEPT; W, M-types), ±1,500 Hz (ETS/CEPT, N-types)			
	Usable temperature range		+22°F to +140°F (EIA) –25°C to +55°C (ETS/CEPT, N-types)		+22°F to +140°F (EIA) –20°C to +55 C (ETS/CEPT)	
Dimensions (proj. not incl.)		57 (W) × 140 (H) × 37 (D) mm ; 2 ¼ (W) × 5 ½ (H) × 1 15/32 (D) in				
Weight (with BP-196)		390 g ; 13.8 oz				
TRANSMITTER	Output power		High 5 W Low 1 W	High 4 W Low 1 W		
	Modulation system		Variable reactance frequency modulation			
	Max. frequency deviation		±5.0 kHz (W-type), ±4.0 kHz (M-type), ±2.5 kHz (N-type)			
	Spurious emissions		70 dB typ. (EIA) 0.25 µW (ETS/CEPT)			
	Adjacent channel power		70 dB (W-type, M-type) 60 dB (N-type)			
	Transmitter audio distortion Hum and noise		Less than 5 % at 1 kHz, 60 % deviation			
	EXT MIC. connector		3-conductor 2.5 (d) mm (1/10") / 2 kΩ			
RECEIVER	Receive system		Double-conversion superheterodyne system			
	Intermediate frequencies		1st 31.050 MHz 2nd 450 kHz	1st 46.350 MHz 2nd 450 kHz		
	Sensitivity (typical)		0.25 µV for 12 dB SINAD 0.63 µV (emf) for 20 dB SINAD		0.3 µV for 12 dB SINAD 0.79 µV (emf) for 20 dB SINAD	
	Squelch sensitivity (at threshold; typical))		0.25 µV		0.3 µV	
	Adjacent channel selectivity		70 dB (W-type) 60 dB (N-type)			
	Spurious response rejection ratio		70 dB			
	Intermodulation rejection ratio		65 dB			
	Audio output power (at 9.6 V DC)		500 mW (typ) at 10 % distortion with an 8 Ω load			
	EXT SP connector		3-conductor 3.5 (d) mm (1/8") / 8 Ω			

Measurements made in accordance with EIA/TIA-152-C, 204D, 603 or ETS-300-086 or CEPT T/R 24.
All stated specifications are subject to change without notice or obligation.

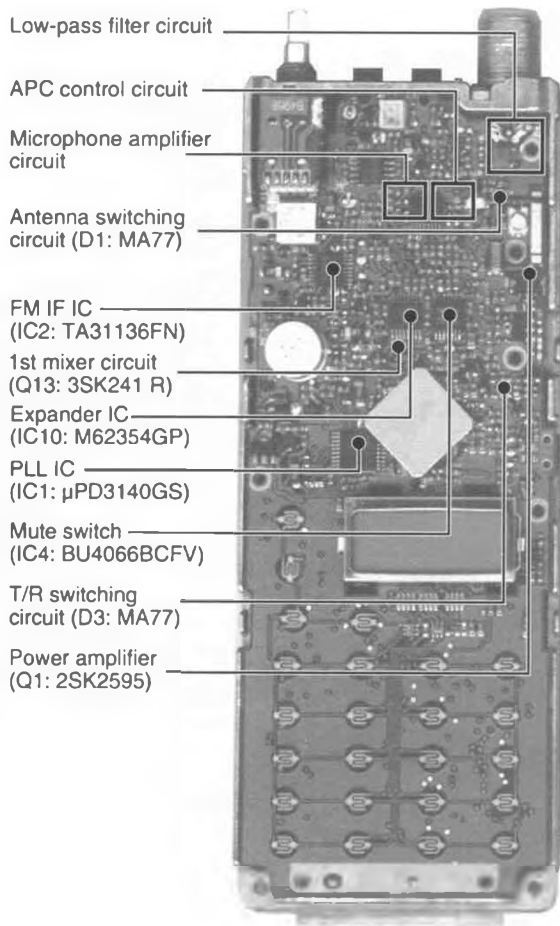
TOP VIEW



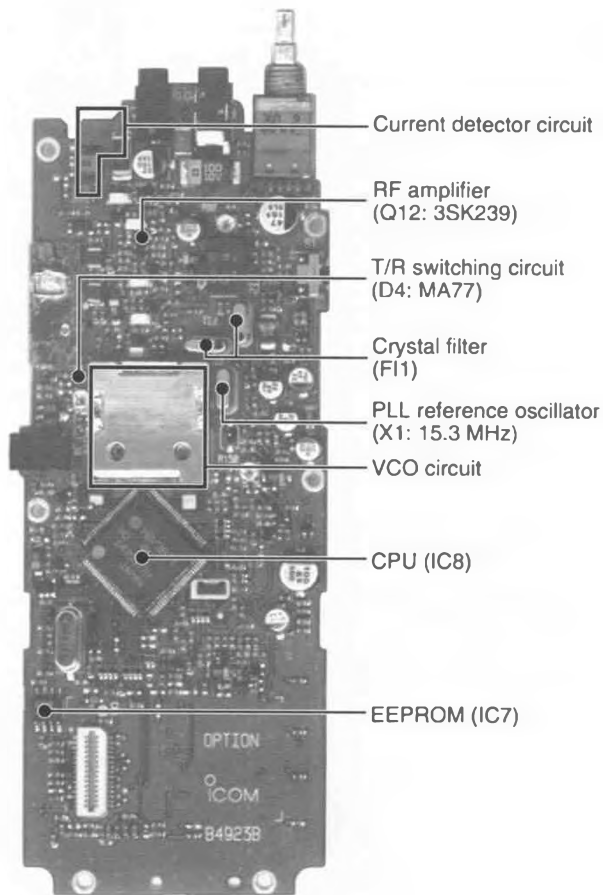
BOTTOM VIEW

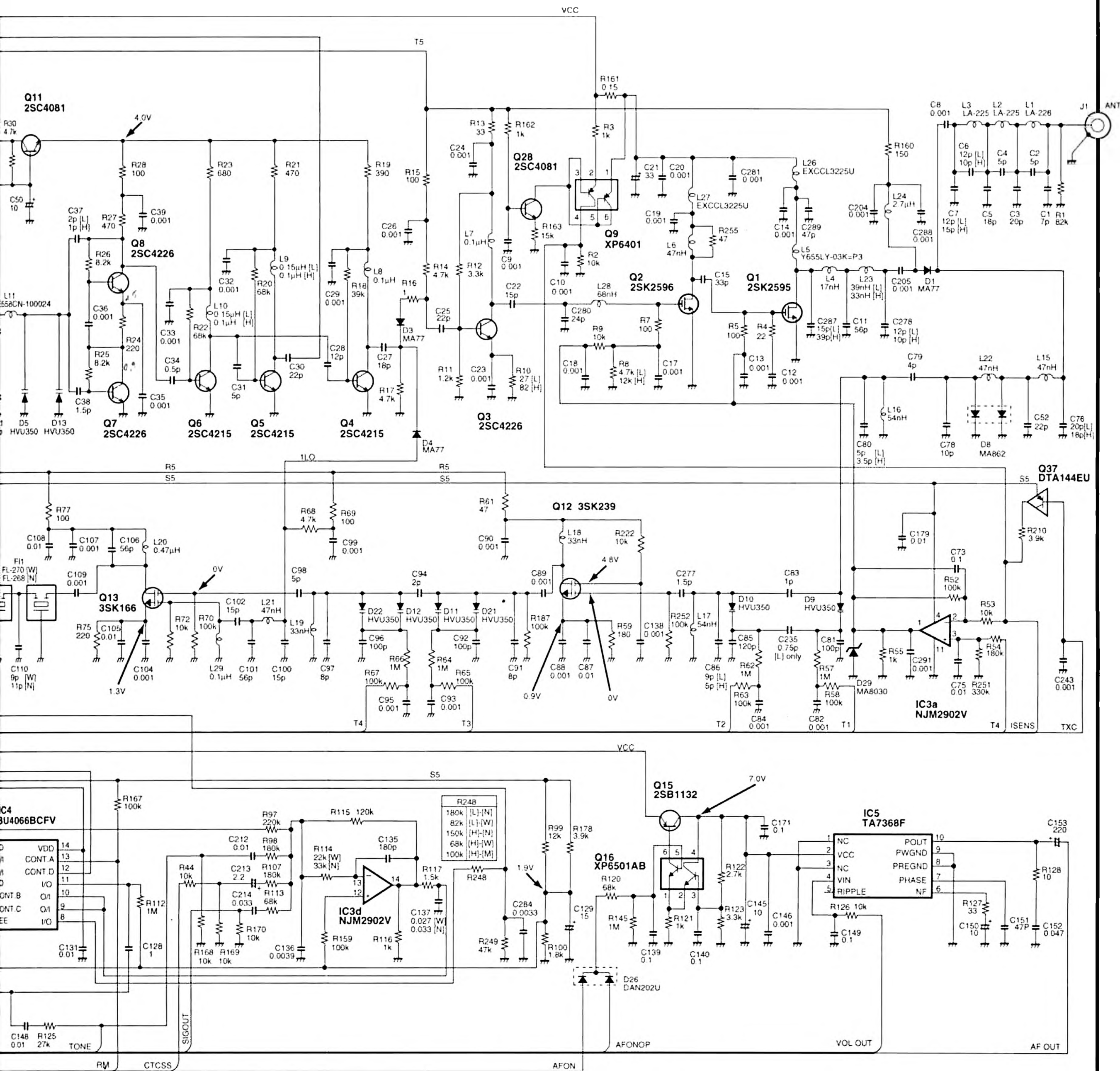


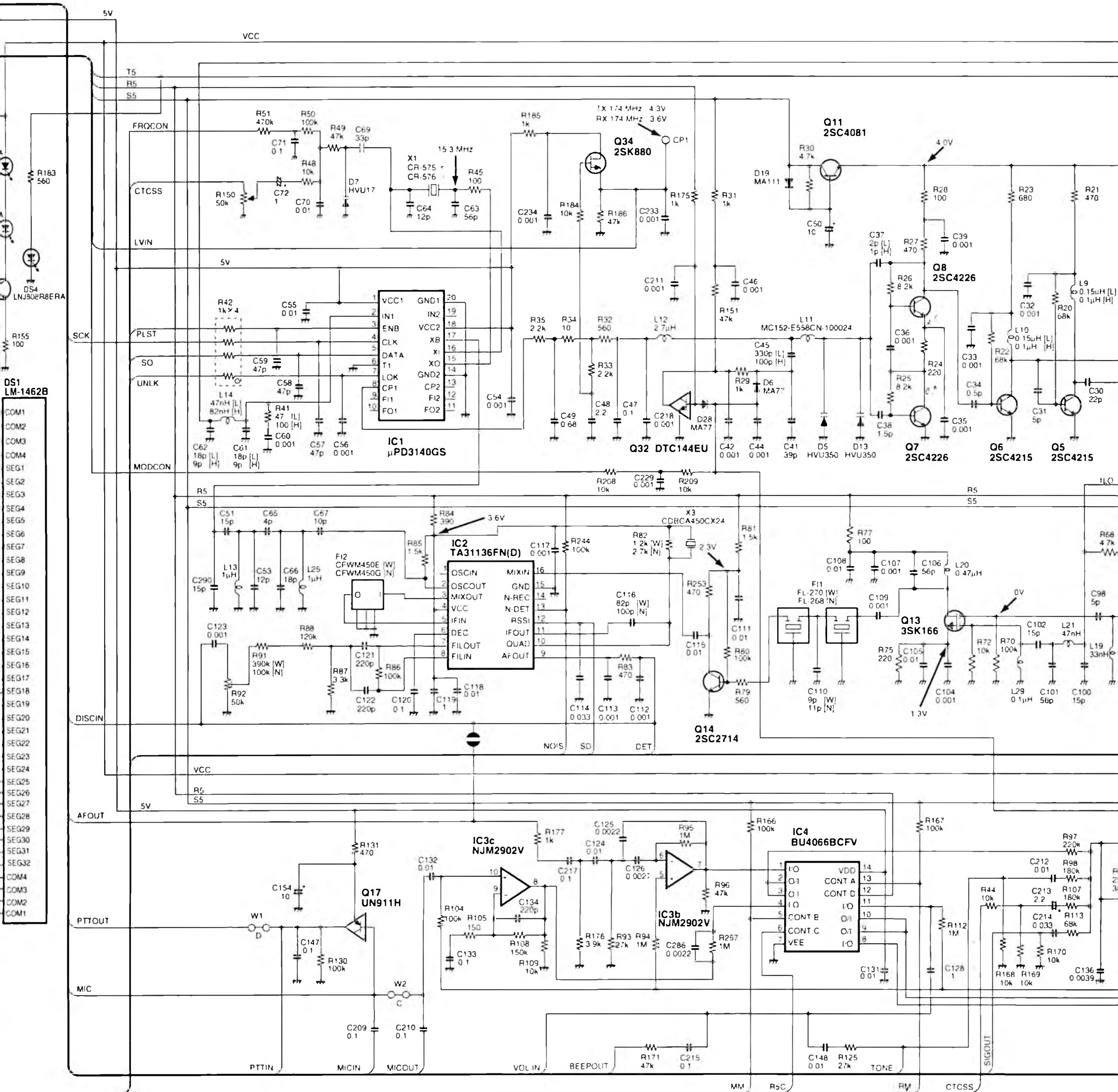
TOP VIEW

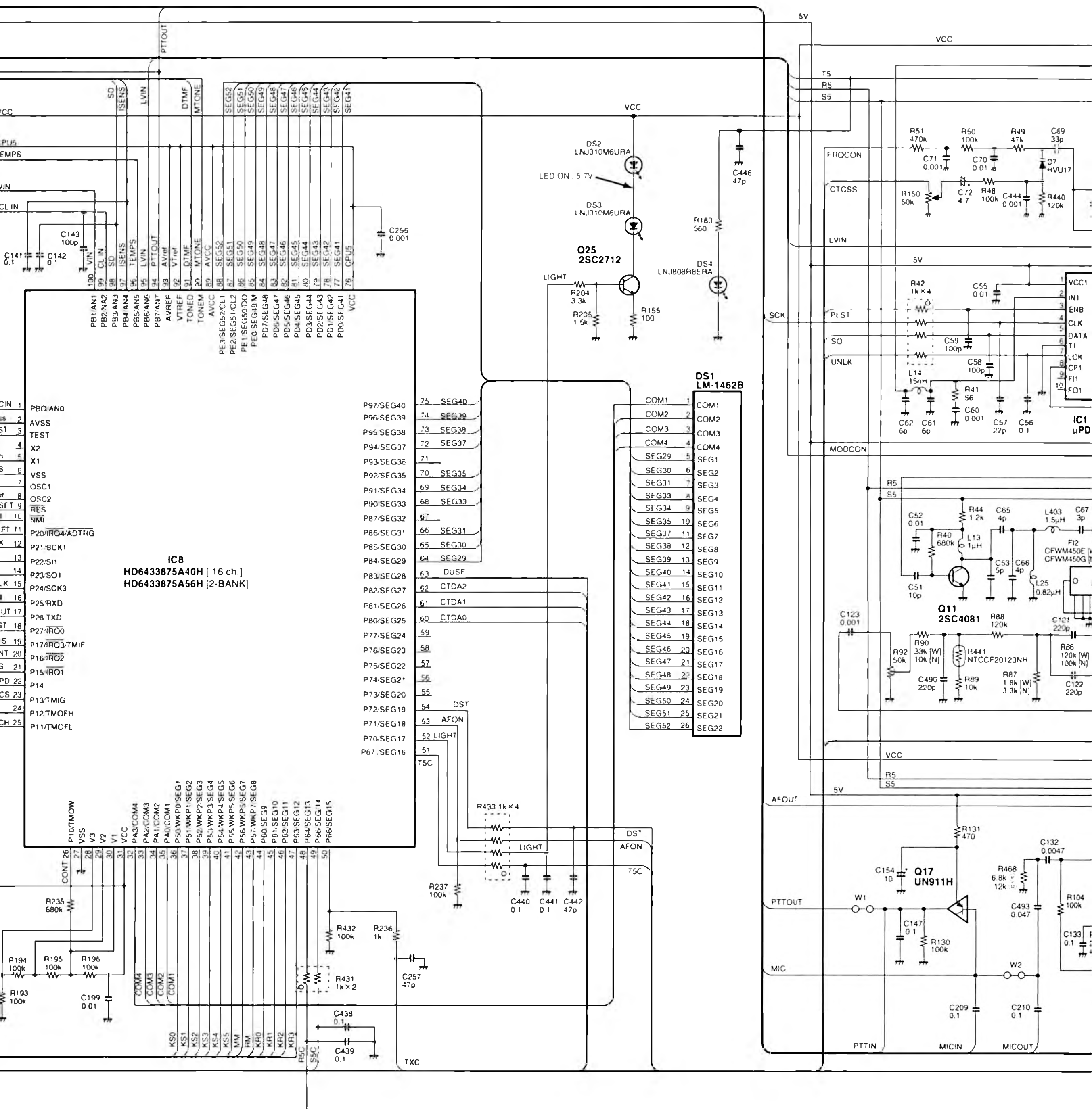


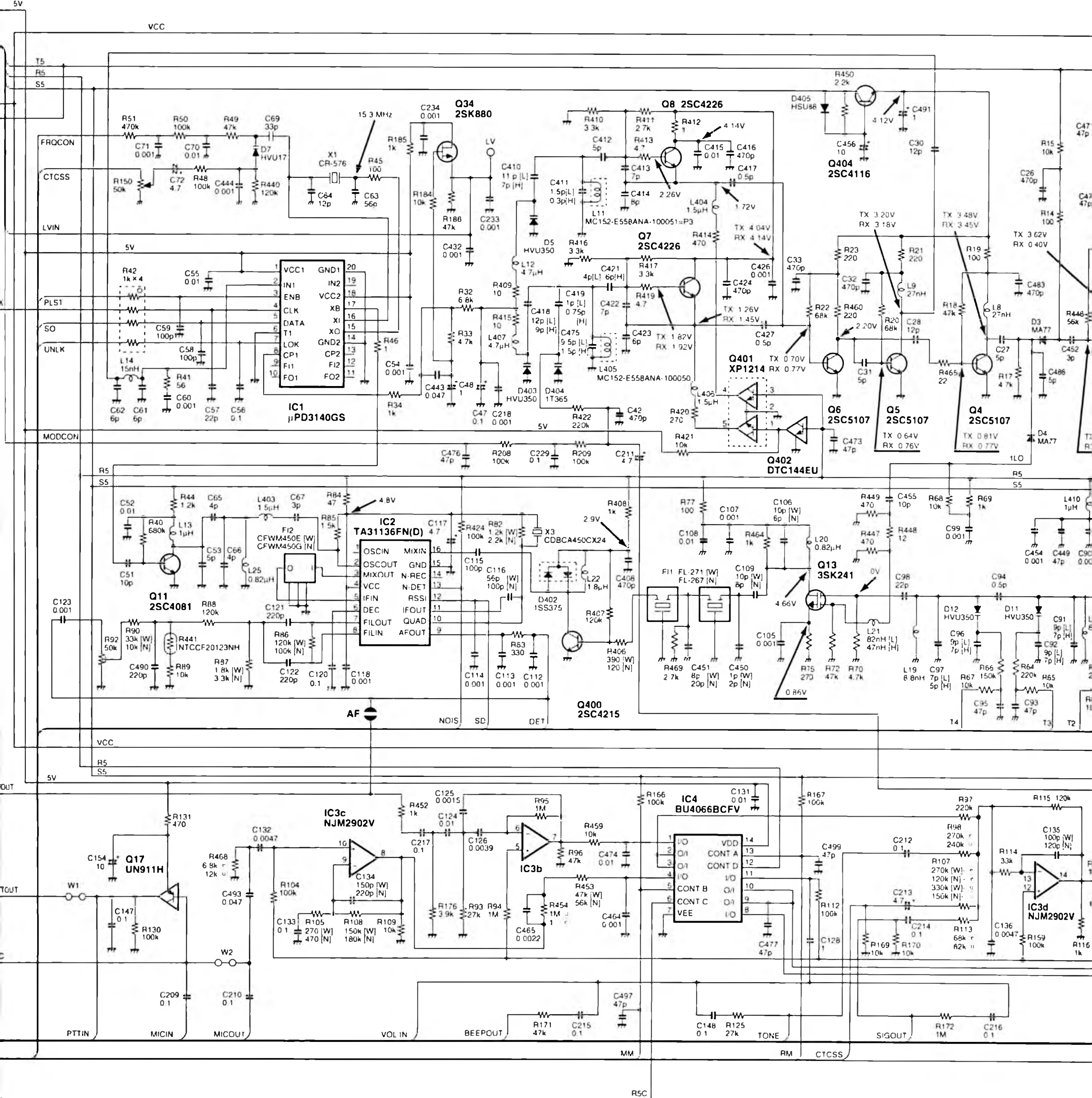
BOTTOM VIEW

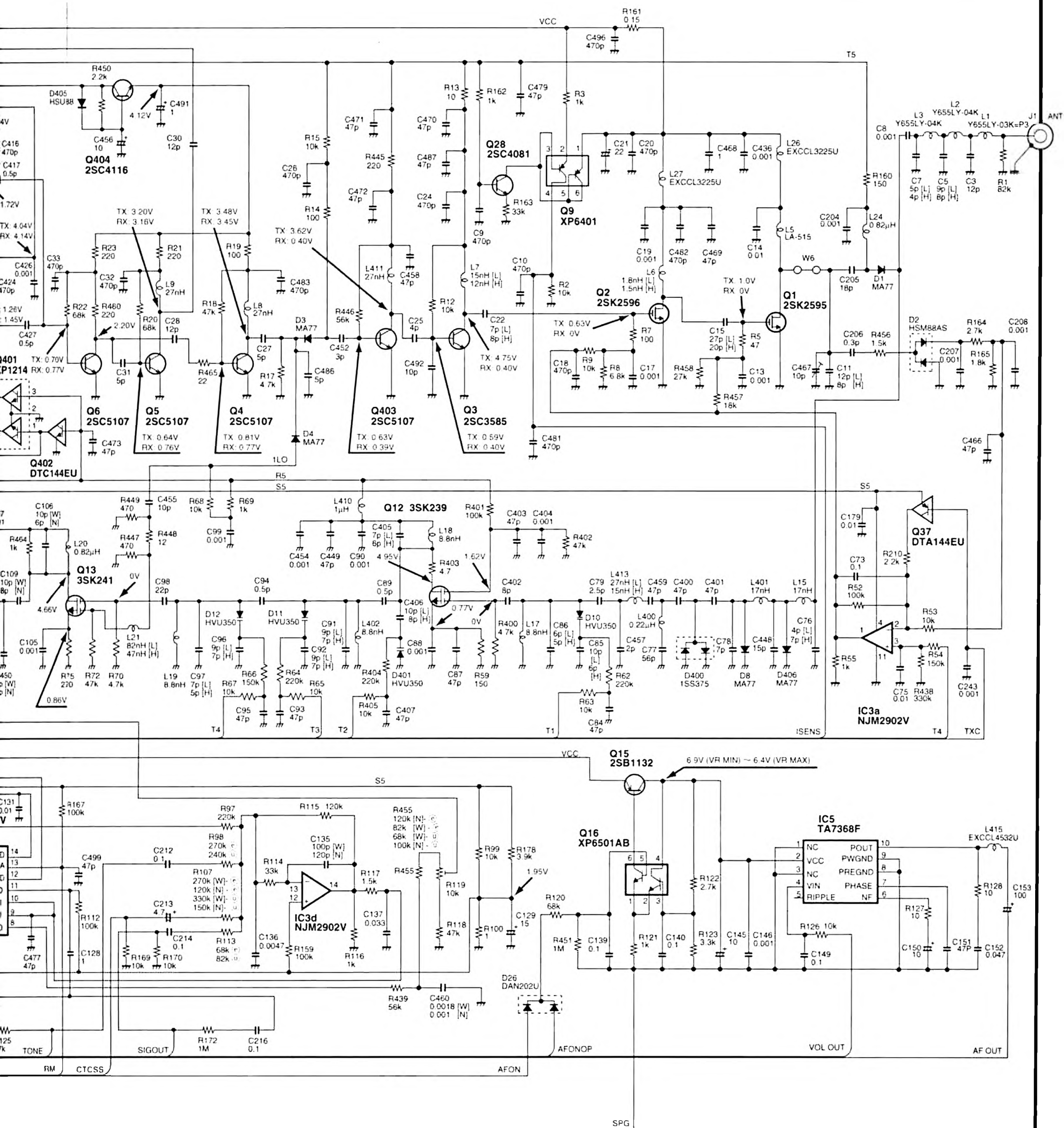


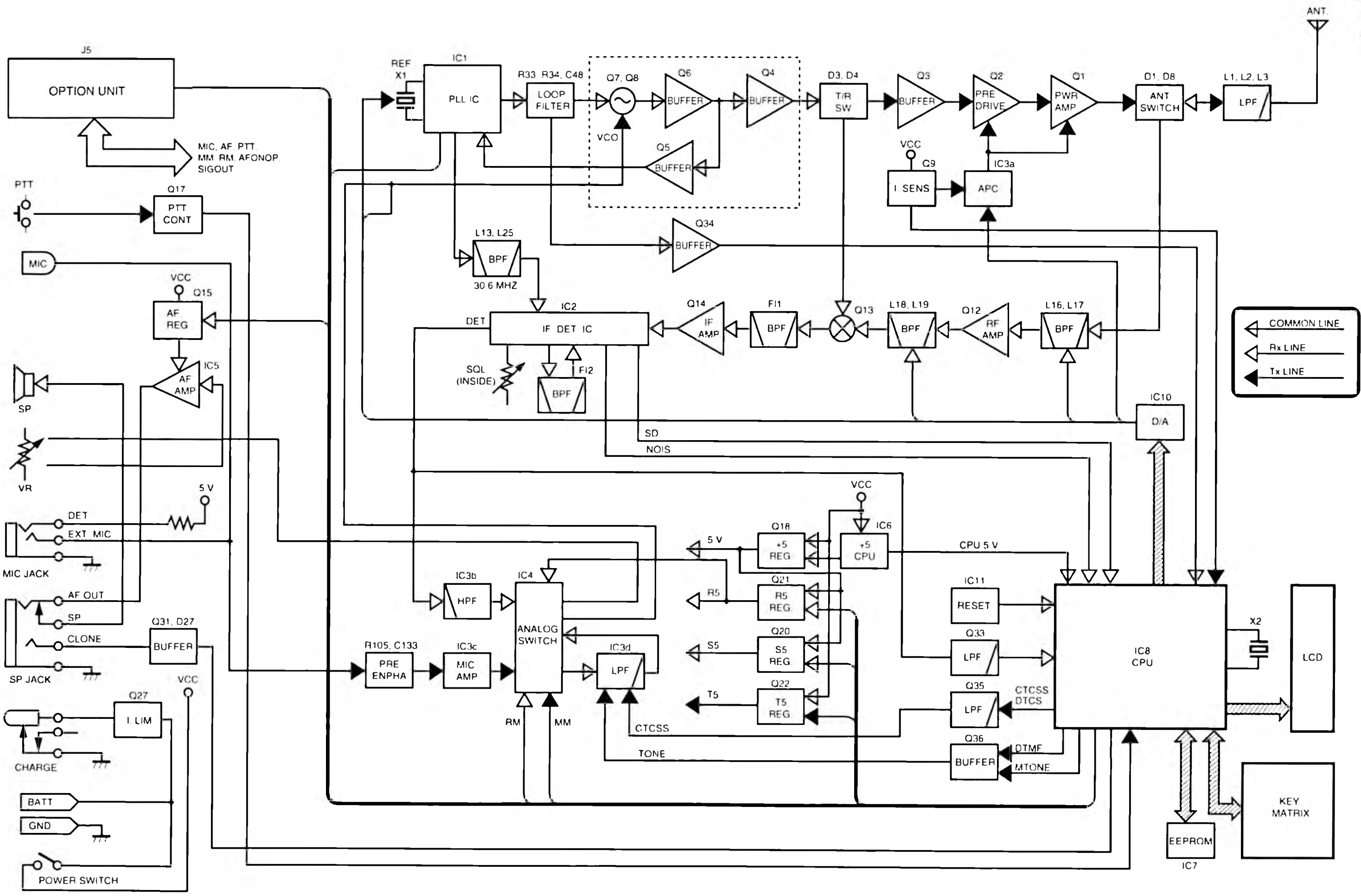


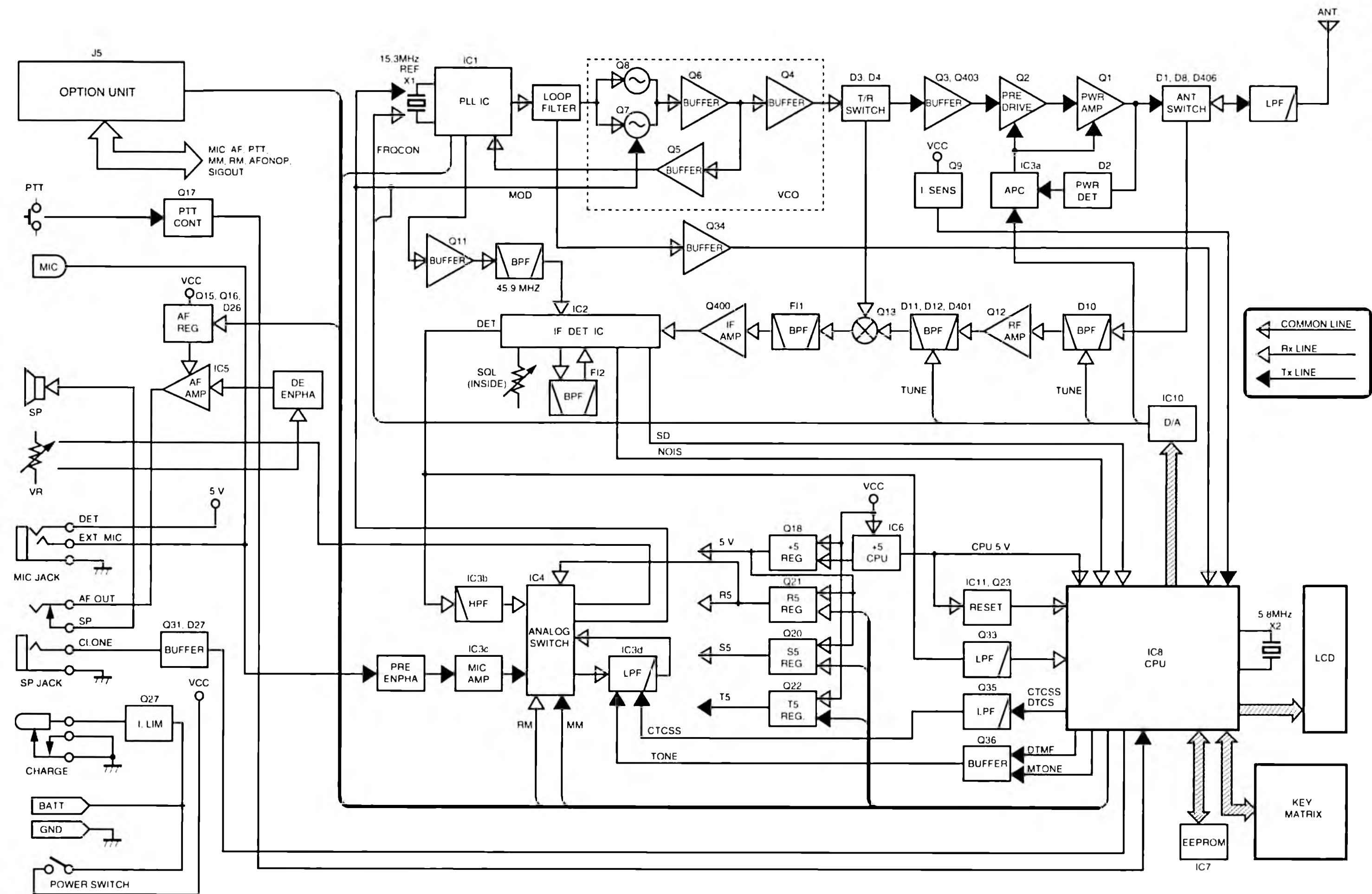












4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT

Received signals are passed through the low-pass filter (L1–L3, C1–C7 for IC-F3/S, L1–L3, C3, C5, C7 for IC-F4/S). The filtered signals are applied to the $\lambda/4$ type antenna switching circuit (D8 for IC-F3/S D406, D8 for IC-F4/S).

The antenna switching circuit functions as a low-pass filter while receiving. However, its impedance becomes very high while D8 (IC-F3/S)/D406 and D8 (IC-F4/S) is/are turned ON. Thus transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a $\lambda/4$ type diode switching system. The passed signals are then applied to the RF amplifier circuit.

4-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit are amplified at the RF amplifier (Q12) after passing through the tuneable bandpass filter (D9, D10, C83 for IC-F3/S, D10, L413, C79 for IC-F4/S). The amplified signals are applied to the 1st mixer circuit (Q13) after out-of-band signals are suppressed at the tuneable bandpass filter (D11, D12, D21, D22, C94 for IC-F3/S, D11, D12, D401, C94 for IC-F4/S).

Varactor diodes are employed at the bandpass filters that track the filters and are controlled by the CPU (IC8) via the expander IC (IC10) using T1–T4 signals. These diodes tune the centre frequency of an RF passband for wide bandwidth receiving and good image response rejection.

4-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will be passed through a crystal filter at the next stage of the 1st mixer.

The signals from the RF circuit are mixed at the 1st mixer (Q13) with a 1st LO signal coming from the VCO circuit to produce a 31.05 MHz (IC-F3/S) or 46.35 MHz (IC-F4/S) 1st IF signal.

The 1st IF signal is applied to a pair of crystal filters (F11) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q14 for IC-F3/S, Q400 for IC-F4/S), then applied to the 2nd mixer circuit (IC2, pin 16).

4-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC2, pin 16), and is mixed with the 2nd LO signal to be converted to a 450 kHz 2nd IF signal.

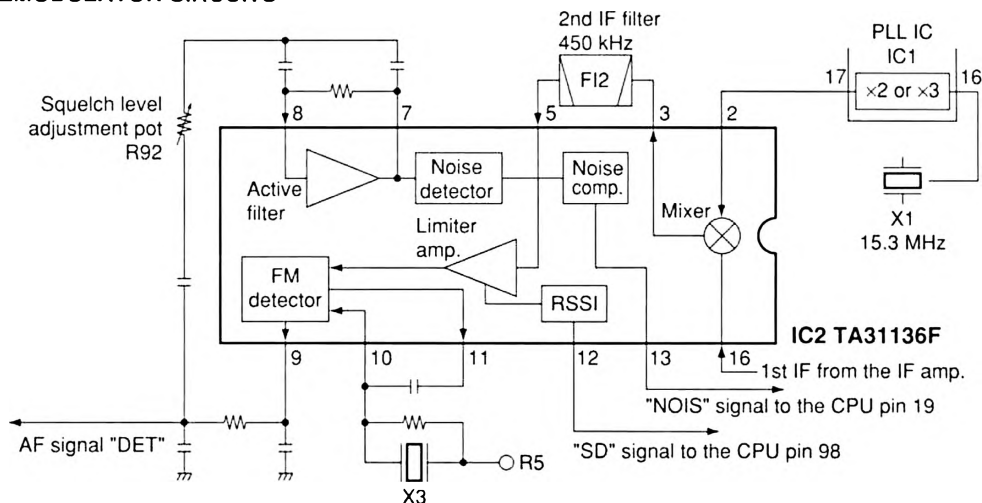
The FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 2nd LO signal (30.6 MHz for IC-F3/S, 45.9 MHz for IC-F4/S) is produced at the PLL circuit by dividing it's reference frequency.

The 2nd IF signal from the 2nd mixer (IC2, pin 3) passes through a ceramic filter (F12) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC2, pin 5) and applied to the quadrature detector (IC2, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

4-1-5 AF CIRCUIT

AF signals from the FM IF IC (IC2 pin 9) are applied to the mute switch (IC4, pin 1) via the AF filter circuit (IC3b, pins 6, 7). The output signals from pin 11 are applied to the AF power amplifier (IC5, pin 4) after being passed through the [VOL] control (VR board, R1).

•2nd IF AND DEMODULATOR CIRCUITS



The signal output from the current sensor circuit (Q9, Q28; IC-F3/S) or the power detector circuit (D2; IC-F4/S) is applied to the differential amplifier (IC3a, pin 2), and the “T4” signal from the expander (IC10, pin 14), controlled by the CPU (IC8), is applied to the other input for reference.

When the driving current is increased, input voltage of the differential amplifier (pin 2) will be increased. In such cases, the differential amplifier output voltage (pin 1) is decreased to reduce the driving current.

4-3 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

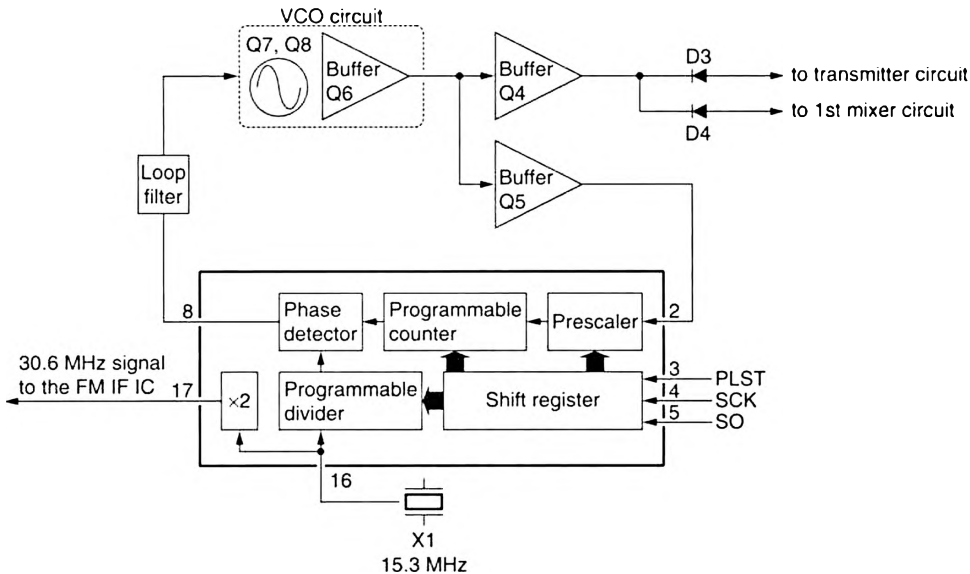
The PLL circuit contains the VCO circuit (Q7, Q8). The oscillated signal is amplified at the buffer-amplifiers (Q5, Q6) and then applied to the PLL IC (IC1, pin 2).

The PLL IC contains a prescaler, programmable counter, phase detector and charge pump, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

A portion of the VCO signal is amplified at the buffer-amplifier (Q4) and is then applied to the receive 1st mixer or transmit buffer-amplifier circuit via the T/R switching diode (D3, D4).

• IC-F3/S PLL circuit



4-4 POWER SUPPLY CIRCUITS

VOLTAGE LINE

Line	Description
HV	The voltage from the attached battery pack.
VCC	The same voltage as the HV line (battery voltage) which is controlled by the power switch ([VOL] control).
CPU5	Common 5 V converted from the VCC line by the reference regulator circuit (IC6). The output voltage is applied to the CPU (IC8) and the 5V regulator circuit.
5V	Common 5 V converted from the VCC line by the 5 V regulator circuit (Q18, Q19) using the reference regulator (IC6).
T5	5 V for transmitter circuits regulated by the T5 regulator circuit (Q22).
R5	5 V for receiver circuits regulated by the R5 regulator circuit (Q21).
S5	Common 5 V converted from the 5V line by the S5 regulator circuit (Q20).
OPT	The same voltage as the 5V line for the optional HM-75A or HS-51 through a resistor (R132).

4-5 CPU PORT ALLOCATIONS

4-5-1 CPU (IC8)

Pin number	Port name	Description
1	CTCIN	Input port for CTCSS/DTCS signals for decoding.
11	CSIFT	Outputs reference oscillator for the CPU control signal.
12	SCK	Outputs clock signal to the PLL IC (IC1), EEPROM (IC7) and expander IC (IC10), etc.
13	SI	Input port for the data signals from EEPROM (IC7), etc.
14	SO	Outputs data signals to the PLL IC (IC1), EEPROM (IC7) and expander IC (IC10), etc.
15	UNLK	Input port for PLL unlock signal from the PLL IC (IC1). High level signal is applied during unlock.
18	PLST	Outputs strobe signals to the PLL IC (IC1).
19	NOIS	Input port for noise signals (pulse type) from the FM IF IC (IC2).
26	CONT	Outputs LCD contrast control signal. High: When normal level is selected
36–41 (IC-F3/S)	KS0–KS5	Output ports for key matrix.
40, 41 (IC-F4/S)	KS4, KS5	
42	MM	Outputs mic. mute control signal. Low: When DTMF or 2/5-tone signal is selected
43	RM	Outputs RX mute control signal. Low: When muted
44–47	KR0–KR5	Input ports for key matrix.
48	R5C	Outputs R5 regulator control signal. Low: While receiving
49	S5C	Outputs S5 regulator control signal. Low: While power is ON
50	TXC	Outputs T5 regulator control signal. Low: While transmitting
51	T5C	Outputs T5 regulator control signal. Low: While transmitting
52	LIGHT	Outputs LCD backlight control signal. High: Lights ON
53	AFON	Outputs the regulator circuit for the AF amplifier control signal. High: While AF amp. is activated.
54	DST	Outputs strobe signals to the expander IC (IC10).
60–62	CTDA0–CTDA2	Outputs CTCSS and DTCS encode signals (3-bit, D/A type).
63	DUSE	Outputs filter switch control signal for the CTCSS and DTCS (Q38). High: DTCS is activated.

CPU (IC8) — continued

Pin number	Port name	Description
90	MTONE	Output port for: Beep audio while receiving. 2/5-tone signals while transmitting.
91	DTMF	Output port for DTMF signals while transmitting.

4-5-2 OUTPUT EXPANDER IC (IC10)

Pin number	Port name	Description
2	DST	Input port for strobe signals.
3	SCK	Input port for clock signal.
4	SO	Input port for data signal.
11–13	T1–T3	Output tuneable bandpass filter control voltage.
14	T4	Outputs tuneable bandpass filter control signal while receiving. Outputs RF output power control signals while transmitting.

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 9.6 V DC Current capacity : 5 A or more	Audio generator	Frequency range : 300–3000 Hz Output level : 1–500 mV
RF power meter (terminated type)	Measuring range : 1–10 W Frequency range : 120–500 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Attenuator	Power attenuation : 40 or 50 dB Capacity : 10 W or more
Frequency counter	Frequency range : 0.1–500 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 120–500 MHz Output level : 0.1 μV–32 mV (–127 to –17 dBm)
FM deviation meter	Frequency range : DC–500 MHz Measuring range : 0 to ±5 kHz	DC voltmeter	Input impedance : 50 kΩ/V DC or better
Digital multimeter	Input impedance : 10 MΩ/V DC or better	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
		AC millivoltmeter	Measuring range : 10 mV–10 V

■ TRIMMER ADJUSTMENT

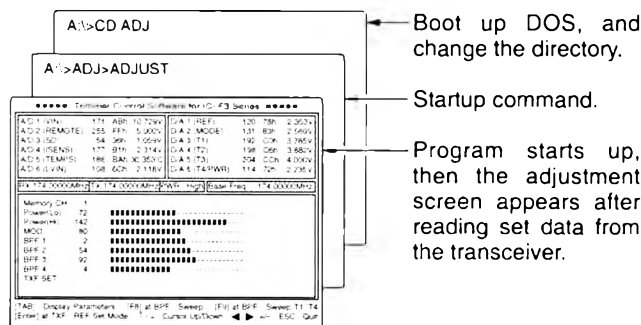
When you adjust the contents on page 5-4 or 5-8, TRIMMER ADJUSTMENT, the optional EX-1961 FIELD PROGRAMMING SOFTWARE (Rev. 2.0 or later) and OPC-478 CLONING CABLE are required.

• STARTING TRIMMER ADJUSTMENT

Turn ON power to the transceiver, connect a computer to the [SP] jack using the optional OPC-478 CLONING CABLE, then start up the "ADJUST" program in EX-1961.

• STARTING THE PROGRAM

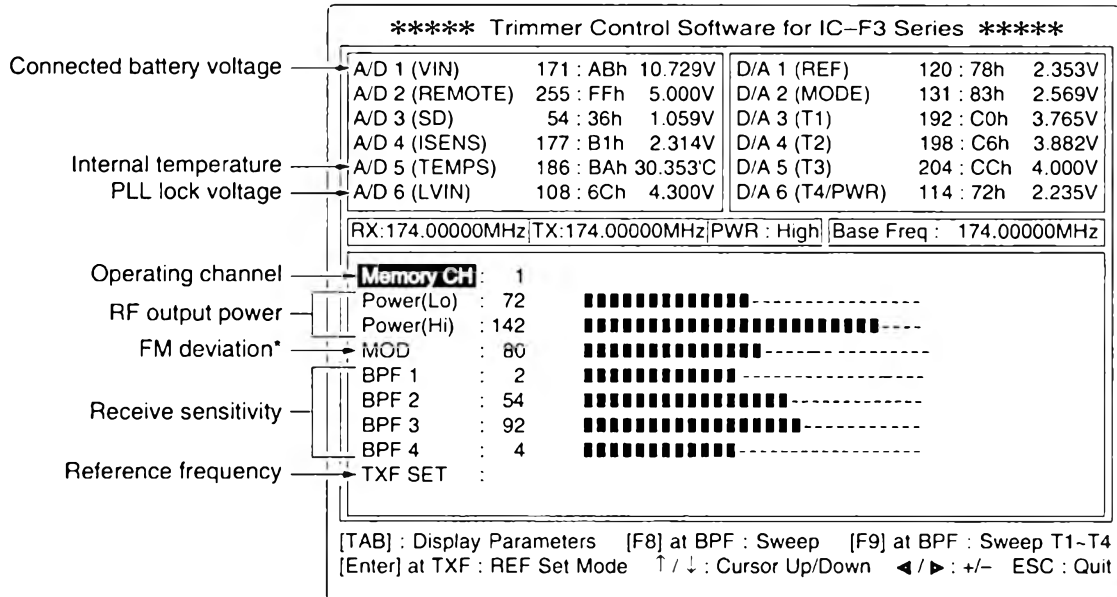
- 1 Boot up DOS.
- 2 Insert the EX-1961 backup disk into drive A.
- 3 Type the following to start up the program:
ADJ>ADJUST [Enter]
 - The adjustment screen appears after reading set data from the transceiver.
- 4 After the adjustment screen appears, set or modify the data as desired.



NOTE: When the EEPROM (IC7) is replaced or the transceiver displays an error message and beeps, the following operation is necessary before starting the ADJUSTMENT.

1. Download the programmed frequency data using the EX-1961 FIELD PROGRAMMING SOFTWARE (Rev. 2.0 or later) from an exact same version of the transceiver, then save it. (See the instructions for detailed operation.)
2. Return to DOS.
3. Copy the saved frequency data into the "ADJ" directory as follows:
A>COPY [file name].ICF A:\ADJ [ENT]
4. Connect the transceiver in which the EEPROM has been replaced, using the OPC-478 CLONING CABLE.
5. Change the directory to "ADJ", and type as follows:
A>CD ADJ [ENT]
A>ADJ>EEPROM [file name].ICF 1* [ENT]
When cloning is successful, the transceiver displays "CL GOOD".

*RS-232C port number. You have to type "A>EEPROM [file name].ICF 2" when the port number is set to "2". This setting can be confirmed in the SETUP window while EX-1961 is running.



NOTE:

The above values for settings are examples only. Each transceiver has its own specific values for each setting.

•DO NOT change the value when adjusting the **IC-F4/S**. A value of 80 is necessary for the IC-F4/S.

• CONNECTIONS

